A 43-Gbps Lithium Niobate Modulator Driver Module

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This paper describes the realization of a 43-Gbps Lithium Niobate modulator driver module. The NRZ driver module utilizes four stages of GaAs pHEMT MMIC amplifiers integrated with an output level detector and feedback loop to provide thermal stability and external control of the output swing. The bias and loop control circuitry are contained in the housing on a PC board external to the sealed MIC section. The integrated module (50.8 x 73.4 x 9.5 mm³) provides 6.0 Vp-p controllable single-ended output voltage while dissipating only 4 watt.

INTRODUCTION

The availability of 43-Gbps Lithium Niobate optical modulators is contributing to the realization of OC-768 optical communication systems, pushing the envelope of today's millimeterwave, modulator driver technology. Besides the high-speed requirement, these modulators need large voltage swings in excess of 5 V_{p-p} to obtain sufficient extinction ratios at 43 Gbps. Previous publications report the use of HEMT [1] and HBT [2] devices to generate large output swings using a push-pull approach. However, utilizing this technology requires the development of advanced module design techniques and control circuitry to meet the requirements of the future's optical communication systems. We believe that this paper is the first presentation of a top-level module (shown in Fig. 1) with advanced bias and control circuitry to provide 6.0 Vp-p output voltage swing and time-domain performance at 43 Gbps for OC-768 optical communication systems. The module design and function are described here accompanied by the measured performance.

CIRCUIT DESIGN

The main objective for the module design is to achieve an output voltage swing of 6 Vp-p in a 50-ohm system with the broadest gain band possible. The reference frequency for the power calculation is 26 GHz where the corresponding CW output power level is approximately equal to +19.5 dBm. To have the maximum amount of system flexibility, the module is also required to handle a range of input levels (to accommodate different multiplexer designs) and a controllable output level (to accommodate and/or optimize the drive for different modulators).

In approaching these challenging targets, the primary consideration is to determine the system budget and line up requirements. The gain in the data path can be achieved with linear or non-linear (compressed) amplification. With a linear gain approach, less amplification stages are required, but the bandwidth flatness is more difficult to maintain with so many passive and active components and interconnections. The linear approach is also more thermally sensitive since the active component gain varies more over temperature in linear mode than when the devices are compressed.

For the non-linear approach, more gain stages are required since the compressed gain is less than the linear gain. The compressed approach provides several advantages: (a.) the flatness is improved as the devices saturate, (b.) a saturated output offers better output signal stability, (c.) the eye diagram becomes more open as the final devices in the final stages compress, and (d.) controlling the compression in each of the last two stages provides a means to control the voltage crossing point. This module design consists of four stages where the first two stages operate in linear mode and the last two stages operate in compression. The resulting module block diagram is shown in Fig. 2.

The data path of the module consists of four stages of 50 kHz-to-40 GHz broadband amplifier circuits to provide the necessary compression and phase inversion for the NRZ signal. Each stage consists of a distributed cascode amplifier MMIC (previously described in [3]) with off-chip bypass components to maintain the gain flatness at lower frequencies. Each of these independent stages is cascaded and has broadband DC blocking capacitors at their input and output. Where required, a broadband coil is used to apply bias to the transmission line with minimal disruption to the data path. The final stage is followed by a broad band, power-sampling circuit. These high frequency components are all contained in a sealed brass package (MIC) with 2.4 mm connectors at the data input and output ports which have EM-simulated transitions to the microstrip transmission line in the MIC.

In the module housing, external to the MIC section, a PC board is used to carry the bias regulation, level feedback, and control circuitry. The power-sampling output voltage is sent through a low-pass filter and buffer amplifier to where it is compared to the externally applied control voltage. The gain control loop provides output signal level stability over temperature. It is structured such that, as the control voltage is increased, the output drain voltage is also increased by the comparing circuit output until the new control voltage is equaled by the amplified detector output. The comparing circuit output signal is also "added" with an externally applied modulation voltage so that an envelope signal tone can be superimposed upon the data for active bias control. An additional external control voltage is applied to the third amplifier through a buffer stage to influence the voltage crossing point of the data.

The complete module is contained in a housing measuring 50.8 x 73.4 x 9.5 mm³ with female and male 2.4 mm connectors at the data input and output ports, respectively. The control voltages, including the output control level, modulation input voltage and crossover control voltage, are all applied through a DC multi-pin connector along with the +10 V (~370 mA) and –10 V (20 mA) power supplies. The total power dissipation is approximately 4 watt.

The most challenging portion of the design rests in accommodating many applications. In order to accomplish this goal, many different levels of input power must be considered (eye amplitude of 320 to 630 mVp-p), and the output power level is controllable (voltage amplitude of 4.5 to 5.8 Vp-p) for each condition including temperature variation. The difficulty does not lie in controlling the output over the large target range, since the loop control circuitry can effectively maintain a range of power levels depending upon the applied control voltage. The challenge rests in optimizing the gain and power of each stage over the large range of operating conditions to prevent over-compression of each stage. If the input power level exceeds that allowable by the MMIC, over-compression results, and the long-term reliability is compromised. By optimizing the bias over the full range of conditions, the maximum power input to each stage is controlled. It is critical to perform this optimization while confirming the 43 Gbps time-domain performance to ensure that the bias, used to limit each stage's input power, does not degrade the eye diagram.

RESULTS

The complete module was evaluated in a 43-Gbps time-domain evaluation set up shown in Fig. 3. An SHF bit pattern generator provided the pseudo-random bit sequence (PRBS) input voltage signal, where an

external 21.5 GHz reference tone was injected as the clock. Discrete attenuator pads were used to control the input power level over a range in eye amplitude from 320 to 630 mVp-p. The output of the module was connected to an Agilent Digital Communications Analyzer through 26 dB of attenuation. The reference input signal is measured by removing the DUT and 20 dB of attenuation from the output, leaving 6 dB and any additional attenuation required to set the input signal.

The results are shown in Fig. 4 and Fig. 5 for the input eye amplitudes of 320 and 630 mV, respectively, and the operating temperature is +25°C. Each of the figures shows the input signal to the driver module and the corresponding output signals when the output voltage amplitude is adjusted to 4.0 and 6.0 V, respectively. As described in the circuit design section, the external control voltage (Vctl) is used to set the output voltage amplitude. For Vctl = 3.1 V, the output voltage amplitude is 6.0 Vp-p (Eye Amp = 5.6 Vp-p); and for Vctl = 1.9 V, the output voltage amplitude is 4.0 Vp-p (Eye Amp = 3.6 Vp-p). The crossover voltage (Vcov) is adjusted to optimize the crossing percentage. The two figures show that the eye S/N is improved, relative to the input signal, for the large variety of operating conditions.

A common rule of thumb is that the bandwidth for a 43-Gbps NRZ driver module should meet or exceed 32 GHz. This rule is derived from the frequency spectrum of the PRBS signal in the data path. In the ideal case, the spectrum is composed of many frequency components which extend from nearly DC to a null at 43 GHz, with the spectral density depending upon the PRBS sequence length. A second grouping of lower magnitude components extends from 43 to 86 GHz. Examination of the input signals shown in Fig. 4 and Fig. 5 reveal that the module input signal is not ideal. The eyes have triangular peaks and valleys due to the length of the rise and fall times that are consistent with a PRBS signal with the higher frequency components rejected. In present systems, it is difficult to maintain the amplification of such high frequency components for the module input signal. In this case, the module amplification at these higher frequencies is less critical. Fig. 6 shows the module presented has a –3 dB large signal bandwidth extending from 50 kHz to 26 GHz. Although the bandwidth is limited, the time-domain performance is very good over many conditions due to the flat magnitude and phase response over the band.

CONCLUSION

This paper described the design and measured performance of a 43-Gbps LN modulator driver module. The amplifier module is designed for external bias control of the output voltage amplitude and crossing point. An external modulation tone can be

applied and superimposed upon the data signal for active bias control. The authors believe this to be the first amplifier module presented which provides controllable 6 Vp-p output voltage swing and good time-domain performance over a broad range of operating conditions for use in OC-768 communications systems.

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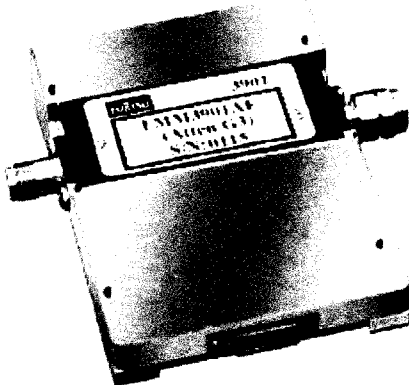
Figure 1. Photograph of the LN driver module. The RF section of the module contains the MMIC amplifiers and high frequency components. The bias and loop control circuitry are provided on a PC board within the housing.
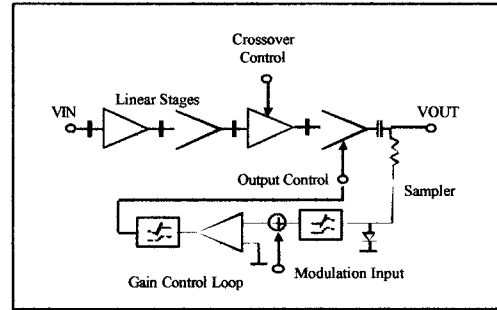

Figure 2. Block diagram of the LN driver module. The RF section is composed of four stages of broadband amplification. A feedback loop from the output detector is used to externally inject a modulation tone and control output voltage level.
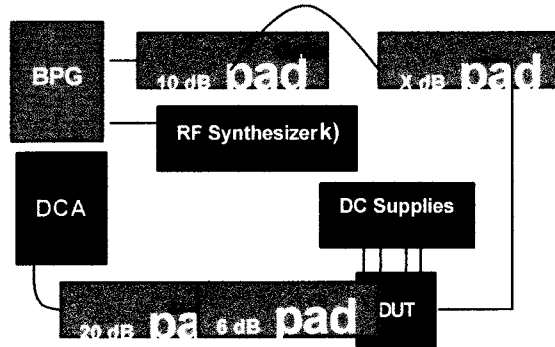

Figure 3. Test set-up for 43-Gbps time domain testing. An X dB pad is used for discrete input power control. The 26-dB attenuation at the output is to protect the DCA and is electronically removed from the measurement.

Lower Input Signal Voltage

Scale: 100 mV/div
Crossing = 48.3%
Jitter RMS = 1.90 ps
Eye S/N = 6.93
Eye Amp = 320 mV

Output Signal Voltage (Vctl = 1.9 V, Vcov = 2.0 V)

+10 V (350 mA)
-10 V (20 mA)
Scale: 1.5 V/div
Crossing = 50.7%
Jitter RMS = 2.04 ps
Eye S/N = 8.43
Eye Amp = 3.6 V
Voltage Amp = 4.0 V

Output Signal Voltage (Vctl = 3.1 V, Vcov = 0 V)

+10 V (390 mA)
-10 V (20 mA)
Scale: 1.5 V/div
Crossing = 50.9%
Jitter RMS = 2.09 ps
Eye S/N = 7.27
Eye Amp = 5.6 V
Voltage Amp = 6.0 V

Figure 4. Measured input (320 mV) and output 43 Gbps eye diagrams of two different bias conditions for the driver module

Higher Input Signal Voltage

Scale: 150 mV/div
Crossing = 47.5%
Jitter RMS = 1.98 ps
Eye S/N = 6.97
Eye Amp = 630 mV

Output Signal Voltage (Vctl = 1.9 V, Vcov = 2.0 V)

+10 V (340 mA)
-10 V (20 mA)
Scale: 1.5 V/div
Crossing = 48.5%
Jitter RMS = 1.97 ps
Eye S/N = 8.93
Eye Amp = 3.6 V
Voltage Amp = 4.0 V

Output Signal Voltage (Vctl = 3.1 V, Vcov = -0.1 V)

+10 V (380 mA)
-10 V (20 mA)
Scale: 1.5 V/div
Crossing = 50.8%
Jitter RMS = 1.95 ps
Eye S/N = 8.26
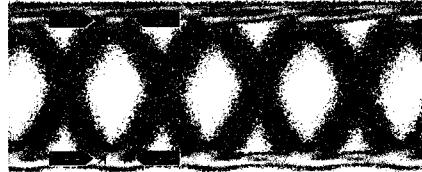Eye Amp = 5.6 V
Voltage Amp = 6.0 V

Figure 5. Measured input (630 mV) and output 43 Gbps eye diagrams of two different bias conditions for the LN driver module
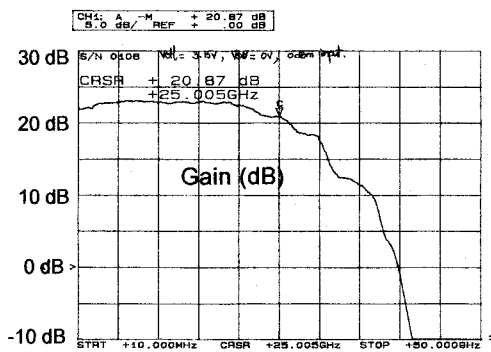

Figure 6. Measured large-signal gain vs. frequency for 0 dBm input power (Vctl = 3 V, Vcov = 0 V)