A 15 GHz LOW COST WIRELESS TRANSCEIVER

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Abstract - This paper reports the investigation on a low cost transceiver for use in point-to-point wireless infrastructure systems operating in the frequency range 14.2 to 15.4 GHz. The issues and tradeoffs encountered when designing a high frequency radio on soft board materials are thoroughly discussed and the main experimental results are presented. A direct modulation system is used in the transmitter, which is capable of delivering an output power of + 22 dBm. The receiver noise figure is better than 3.6 dB with a conversion gain of 20.0 dB.

1.0 INTRODUCTION

The realization of a product on soft board requires a design that is compatible with the limitations from such a material to become successful. An important issue on soft board is the circuit repeatability that is poor compared to thin film. Among the reasons are the dispersions on microstrip impedance, originating from fluctuations in line widths due to etching and copper granulation, dispersions on multilayer chip capacitors and dispersion on the parameters of the packaged active devices. The latter are due to variations in the manufacturing process and their effect on the circuit performance is more pronounced at high frequencies due to the package parasitics. Also, in high volume low cost manufacturing there is no control on the device parameters from lot to lot as one can do on a chip environment. Thus, the challenge is how to design under these conditions a low cost radio transceiver that has minimum adjustments on the circuit to meet the specs.

The approach followed to develop this prototype was to divide the task in four steps, starting with the transceiver **system analysis** to define the specs for each building block of the system. The analysis was done on a single frequency, using Microwave Design System (MDS), a software package by Hewlett-Packard, to obtain information on gain, power and spectrum. Then, in the **circuit design** step, each building block was designed by trading off electrical performance, packaged devices, soft boards and low cost components. The crucial step was the **realization and test** of the building blocks to proof they can perform adequately at 15 GHz. The final task was the cascading of all modules into a custom made housing. An **engineering prototype** was obtained after solving the problems resulting from connecting non 50 ohms modules

2.0 TRANSCEIVER SPECIFICATIONS

The transceiver was designed to operate in short haul digital radio links, in point-to-point communications. The modulation scheme is 4 level FSK, thus containing a constant envelope signal, which tolerates non-linear amplification without degradation on the BER. Consequently, the amplifier cost at high frequencies drops considerably when compared to other modulation systems, like QPSK for instance, which require a minimum of 3 dB back off from the P-1dB point[1]. The LO Phase noise can also be somewhat relaxed, as related in the general specifications in table I. The FSK signal is obtained by direct modulation of the transmitter VCO, applying a modulated Nyquist filtered digital data, as high as 45 Mb/s. The drawback of this system is the spectral efficiency which prevents its application where efficiency is critical.

Transmitter		Receiver	
Freq	14.2 - 15.4 GHz	Freq	14.2 - 15.4 GHz
Gain control	20.0 dB	Conversion gain	20.0 dB
Pout sat	20.5 dBm	Noise Figure	6.0 dB
Phase Noise @ 100 KHz	- 80.0 dBc/Hz	Phase Noise @ 100 KHz	- 80.0 dBc/Hz

Table I - Transceiver Specifications

The transceiver contains a LO for the transmitter and a similar one for the receiver giving versatility to the user when designing the radio frequency plan. In order to simplify the design, the transceiver was divided into three major blocks, namely: Downconverter, Local Oscillator and Transmitter Amplifier.

2.1 Downconverter

The basic downconverter schematic is similar to a conventional heterodyne receiver shown in figure 1, where any RF carrier within the receive band is downconverted to a fixed IF centered at 1.35 GHz. The downconverter comprises a LNA, an edge coupled filter for image rejection, a mixer, and an IF amplifier with gain control. A cost effective way to build a LNA is to employ a packaged PHEMT in the first stage for low noise performance and a packaged MESFET in the second for gain and power performance. In this design, the bonding pads required to attach the devices and blocking caps were used to match the amplifier, thus avoiding use of parallel stubs which often introduces instabilities and limit the frequency of operation. This module presented 3.2 dB noise figure with an associated gain of 20.0 dB.

The mixer is of the single balanced type containing a ratrace and a matched pair of low barrier Schottky diodes inserted on a ceramic package. A maximum conversion loss of 6 dB was obtained with such a topology. The bandpass filter is a conventional edge coupled

microstrip filter containing 5 resonators. The IF amplifier is simply two Silicon MMICs with a pin attenuator in between to provide gain control.

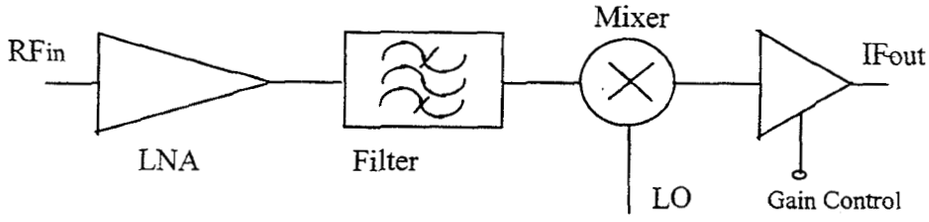

Fig 1. Downconverter schematic

2.2 Local Oscillator

The diagram for the 15 GHz Local Oscillator is illustrated on figure 2. It contains a VCO, a power splitter, two buffer amplifiers, one frequency multiplier and one frequency divider. The resistive power splitter presents only 12 dB isolation that is poor compared to a directional coupler, but it is more compact and additional isolation is obtained by the reverse gain of the buffer amplifiers.

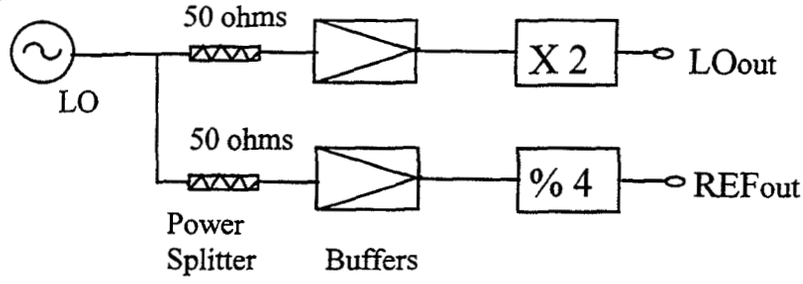

Fig 2. LO schematic

A common collector packaged bipolar device was used as the active element for the VCO. The tank circuit was built with short transmission lines plus a packaged varactor whose parasitics contributed to define the oscillating frequency. The circuit was designed using conventional S-parameter techniques complemented by experimental tuning of the tank circuit in order to optimize the phase noise. The receiver VCO provided + 3 dBm output power within the 6.4 to 7.1 GHz band, with a phase noise better than - 94 dBc/Hz at 100 KHz from the carrier.

The frequency doubler topology is conventional and employs a low cost MESFET in a plastic package. Multiplication gain is in the order of 1.0 dB and the output power is better than + 9.0 dBm. The frequency divider is a digital MMIC and the buffer amplifier is an analogue MMIC, both commercially available on plastic package.

2.3 Transmitter Amplifier

The transmitter amplifier block diagram shown on figure 3, contains a driver amplifier, a power amplifier, and an output detector. At present it is feasible to build a power amplifier with discrete packaged MESFETs, but such approach would require excessive tuning for meeting the specs with consequent labor added. Thus, it was decided to employ two medium power MMICs inserted on a ceramic package. The package was inserted between two ratrace hybrids built on soft board in order to obtain a push-pull amplifier. This approach can be applied due to the good impedance match presented by the MMICs. Besides increasing the power compared to a single ended, it minimizes second harmonic generation and improves amplifier efficiency. The driver amplifier consist of the same module used in the LNA whose bias has been modified to increase gain and power output.

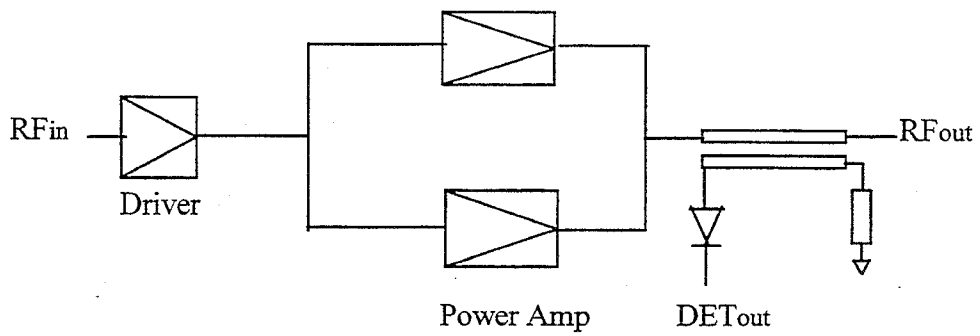

Fig 3. Transmitter amplifier block diagram

One of the requirements for this design was the possibility of controlling the gain over a 20 dB range. It was found that an attenuator using packaged PIN diodes would be too complex to meet this spec on soft board. The low cost alternative was to control gain by changing the drain bias of the transmitter. This was a feasible approach since the driver and power amplifier operate both under saturation, making it possible to control gain with a minimum degradation in the flatness over the band.

3.0 REALIZATION

All circuits were built on a low cost soft substrate type DI-CLAD 880 by ARLON, presenting a dielectric constant of 2.2 and a loss tangent of 0.0009. The choice on substrate thickness was on 10 mils thick in order to improve propagation of 15 GHz signals, and the traces were printed with a width tolerance of +/- 0.5 mils. The substrates were soldered onto standard carriers measuring 0.5 by 1.0 square inches in order to guarantee a good ground plane. The carriers were inserted into a 0.5 inch wide waveguide shown in the photo of figure 4, which presents a cut off frequency of 12 GHz. The DC blocking capacitors are ATC type with tight tolerances, presenting series resonance near the operating frequencies. When all modules were integrated into the housing, there was no moding problems observed due to the use of a

waveguide channel, however absorbers had to be used in the side walls to minimize leakage from Transmitter to Receiver. Independent supply voltage was used for the VCOs to improve phase noise, while + 10 volts and -5 volts was supplied to all other circuits. An automatic bias circuit was used to bias the LNA devices which operate in linear class A mode. That circuit minimizes temperature variations and is able to accomodate a wide dispersion in the FETs DC characteristics.

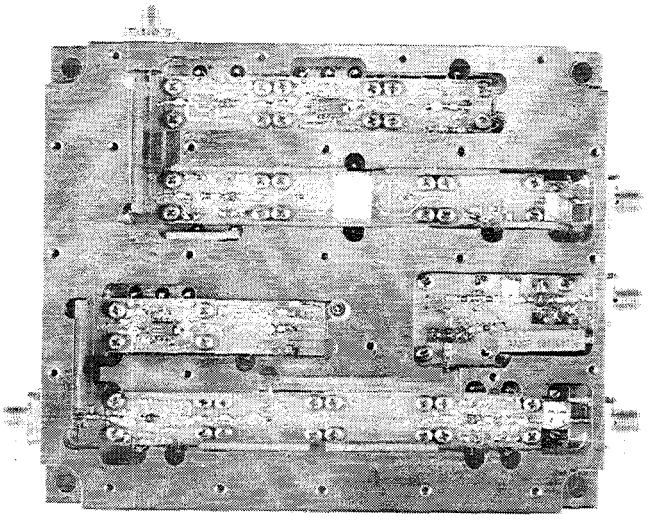

Fig 4. Photo of the complete transreceiver

4.0 EXPERIMENTAL RESULTS

Extensive testing was carried out to verify that the transceiver meet all performance specifications. Testing started at the module level, with each one tested to demonstrate besides electrical performance, ease of manufacture and repeatability. After all subassemblies were tested, they were assembled into the housing, containing independent compartments for the receiver and transmitter. The alignment of the receiver required some tuning to equalize the conversion gain flatness, and adjustments on the IF PIN attenuator to set the receiver gain to 20 dB. The gain performance over temperature is maintained within a 2 dB window, by the use of a temperature dependent pad in the IF path. In the transmitter side there was no need for tuning, since the driver and power amplifier operate under saturation a condition less susceptible to mismatches between modules. Transceiver tests included conversion gain, receiver flatness, output power and phase noise over temperature from -30° C to + 70° C.

The receiver frequency conversion response is shown in figure 5 where a flat 20 dB gain is observed. The image rejection response in also indicated in the same plot, and it is observed a minimum of 40 dB rejection. The indicated phase noise is better than - 88 dBc/Hz over the band. Other important parameters are the noise figure, which is equal to 3.6 dB at room temperature. This parameter changes by +/- 0.5 over the temperature range of -30° C to + 70° C.

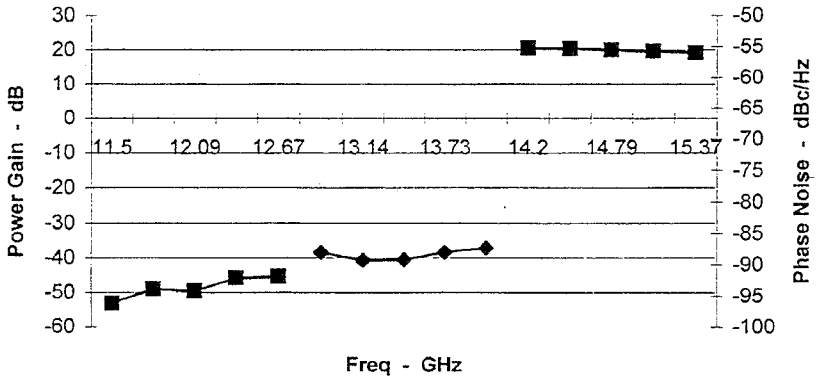

Fig 5. Receiver gain & Phase Noise performance

The measured transmitter saturated output power is shown in figure 6, where it is observed an output power of + 22.0 dBm flat within 0.5 dB all over the transmitter band. The transmitter phase noise is also included in the same figure and is better than -95 dBc/Hz at 100 KHz from the carrier.

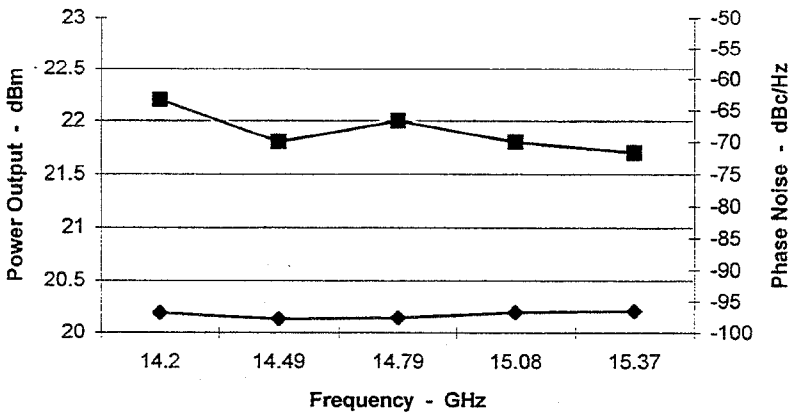

Fig 6. Transmitter Power & phase noise

Spurious signals coming from the LO, multiplier and frequency divider are all under - 40 dBm. The main signal at the output is the second harmonic that is equal to - 38 dBm at the worst point in the band. The gain control as a function of applied bias is represented in figure 7, for the center frequency of operation. It shows a smooth control of the output power for a range greater than 20 dB from the nominal output. The flatness distortion when changing the output power is better than 1 dB all over the band. The control voltage is applied to an inverter and to a current amplifier that bias the amplifiers.

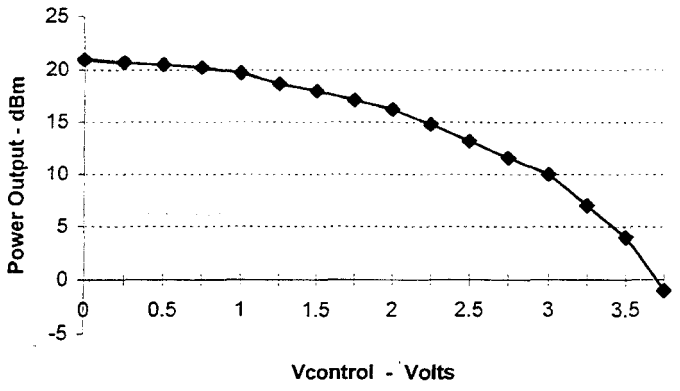

Fig 6. Power output as a function of drain bias.

5.0 CONCLUSIONS

The modular approach followed to design this prototype, proved to be efficient since it was possible to directly detect the limitations of soft board and was easier to find the tradeoffs. A fast turn around time to obtain the hardware and test them on the bench was possible due to the use of a small milling machine to cut the copper traces instead of waiting days to have them done with conventional chemical etching. The experimental results obtained after assembling all modules into a proper housing are comparable to the ones obtained with other technologies, except this is a lower cost alternative. The issue of repeatability that is critical in linear mode of operation and high microwave frequencies is confined in this design to the LNA and MIXER blocks. Other functions are either at lower frequencies where this is less of a problem or on the power amplifier that operate on saturated mode, thus less sensitive to small variations in device parameters.

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