# A HIGH GAIN GaAs MESFET FREQUENCY QUADRUPLER

EDMAR CAMARGO and FATIMA S. CORRERA

LABORATÓRIO DE MICROELETRÔNICA
UNIVERSIDADE DE SÃO PAULO
Cx.P. 8174 - São Paulo-SP - BRAZIL

## ABSTRACT

*This paper presents a comprehensive analysis carried out on a frequency quadrupler from 1 to 4 GHz using a 1 μm dual gate GaAs MESFET. Two different circuit options are proposed, namely with and without feedback. They were constructed on soft substrates and the preliminary microwave results are a + 10 mW output power with a 8.5 dB associated multiplication gain and 6% DC-to-RF power efficiency.*

## INTRODUCTION

In the literature one can find several papers covering the subject of GaAs MESFET frequency multipliers. Recent literature on GaAs MESFET frequency multipliers includes excellent experimental results for low-power frequency doublers,[1,2] and a comprehensive theoretical treatment[3]. However, the majority of these publications deal essentially with frequency doublers. The object of this paper is to study the nonlinear mechanisms involved in the generation of higher order harmonics, and to demonstrate the feasibility of utilizing a dual gate GaAs MESFET as a frequency quadrupler. Two types of circuit have been constructed, with and without feedback, and their performance characteristics are compared and discussed.

## DEVICE SELECTION

Prior to selecting the most appropriate device for the present application, a comparison was made of the performance of single and dual gate GaAs MESFET frequency doublers. Computer simulations[4] showed that the latter presents 6 to 8 dB higher multiplication gain, a result which agrees with experimental published data[1]. Nevertheless, the single gate device delivers more output power for the same drain bias voltage[4]. Since the purpose of this work was to obtain high gain rather than high output power, it was decided to use dual gate GaAs MESFET's in the experiments. In the present context the device used was the DUGAT P106, manufactured by the Plessey Company, which is capable of delivering an output power in the order of 10 mW at 4 GHz.

## ACTIVE FREQUENCY MULTIPLIERS

In a frequency doubler, the second harmonic is generated by inducing at the drain terminal an asymmetric voltage waveform resembling a rectified sinusoid. The second harmonic is extracted by means of a high pass filter which reactively blocks the fundamental frequency. Since higher harmonics are of a very low level, additional filtering is unnecessary. The active rectifying effect is obtained by exploiting simultaneously the device non-linear parameters $g_m$ and $g_d$, which are controlled by the external bias voltages and the fundamental frequency impedance connected to the drain. Optimum operation is obtained when the drain is terminated at the fundamental frequency by a purely reactive circuit, which resonates the transistor's output capacitance [5].

In higher order frequency multipliers, the direct input signal and $g_m$, $g_d$ interaction does not generate the desired harmonic with a reasonable multiplication gain. Thus, additional mechanisms must be used in order to improve the multiplier performance.



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Two procedures are proposed to recover the energy distributed in the several harmonics generated at the drain and convert them to a single desired output harmonic frequency. One way is to reflect all harmonics back to the drain and the other is to feed them back to the input gate.

In the first procedure, the fundamental frequency impedance presented to the drain is the same as in the frequency doubler case. However, the second and higher harmonics are reflected back to the drain except for the output frequency which is terminated in a 50 ohm load. The MESFET nonlinearity causes these harmonics and fundamental to produce higher harmonics. It must be noted that the reactive harmonic terminations must be properly phased so as to enhance the power at the output frequency.

The second proposed procedure to increase the global multiplication gain, is to feedback to the input the harmonics which are present at the output. A basic topology for this circuit is represented in figure 1, which is quite similar to the one proposed in the literature for a feedback frequency doubler[3].

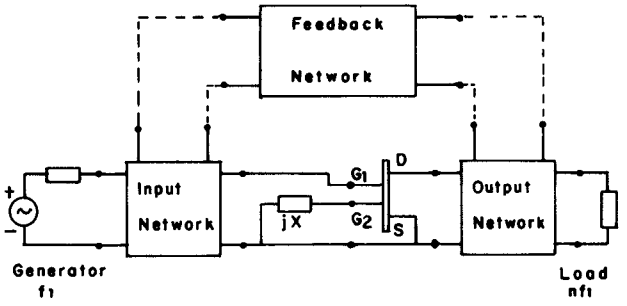


Fig. 1 - GaAs MESFET Frequency Multiplier

To avoid instability problems that often occur in regenerative circuits, the output-to-input coupling was made weak enough to give a loop gain less than unit under any operating conditions. Since the harmonics fed back to the input are of a lower level than the signal furnished by the generator, $P_1$, the following mechanisms contribute to enhance the power of the desired harmonic: power amplification of a sample of the output harmonic (n) and frequency conversion by mixing the (n-1) and/or (n+1) output harmonics with the fundamental frequency. Assuming the ideal case where the phase of the feedback signals are such that all the power terms add up at the output, them the power at the desired $n^{th}$ harmonic, $P_n$, can be represented by the equation:

$$P_n=(1-A_n)[P_1MG + P_nA_nG_n + (P_{n-1}A_{n-1} + P_{n+1}A_{n+1})\ CG] +$$

$$+ \text{ other terms}$$

where,

$P_{n-1}, P_{n+1}$ - Power at the harmonics (n-1), (n+1)

$A_{n-1}, A_{n+1}$ - Power coupling at the harmonics (n-1), (n+1)

In this equation one can identify the three most important mechanisms contributing to a higher global multiplication efficiency. They are:

- Frequency multiplication from the fundamental to the $n^{th}$ harmonic, whose power gain is denoted by MG.
- Large signal amplification of part of the $n^{th}$ harmonic frequency fed back to the input with a power gain $G_n$.
- Frequency conversion resulting from mixing the fundamental frequency with the feedback harmonics (n-1) and (n+1) with a conversion gain represented by CG.

The next step is the design of a test circuit which allows the investigation of each of these terms independently.

## TEST CIRCUIT

The approach used in this paper to design an experimental test circuit starts with the investigation of the transistor stability state. Small signal S-parameters furnished by the manufacturer were used for this purpose. Next, an open loop frequency multiplier can be designed by properly terminating the drain and tuning gate 1 for maximum power transfer at the fundamental frequency. An earlier work[1] showed that the second gate must also be reactively terminated in order to maximize the multiplication gain. Finally, the loop is closed and it is assumed that this action does not affect the former tunning of gate 1 and gate 2. Thus, only the output and feedback circuits need to be adjusted.

According to these steps, a test circuit employing the DUGAT in the P106 package, was designed for multiplying signals from 1 to 4 GHz. This relatively low frequency was used for our tests, so that one has a better control on the circuit parameters. The circuit was implemented in microstrip and slot lines on 25 mil thick high dielectric constant ($\varepsilon_r$ = 10) soft substrate. It is represented as two superposed masks in figure 2. The input network at gate 1 comprises open microstrip stubs for tuning the input impedance at the fundamental frequency. Open microstrip stubs are also used for tuning gate 2. The output network makes use of two microstrip-to-slotline transitions and theirs high pass properties to transfer the generated fourth harmonic to the load. So, the fundamental frequency, the second harmonic and part of the third are reflected back to the drain. A slotline power divider is used to couple part of the output signal to the gate via a slotline phase shifter and another transition to microstrip. A diplexer circuit isolates the generator from the feedback loop, using resonant slots to block the feedback signals and a microstrip band-reject filter to block the fundamental frequency. The selection of the feedback harmonic is obtained by adjusting the transition coupling and the open microstrip stubs.

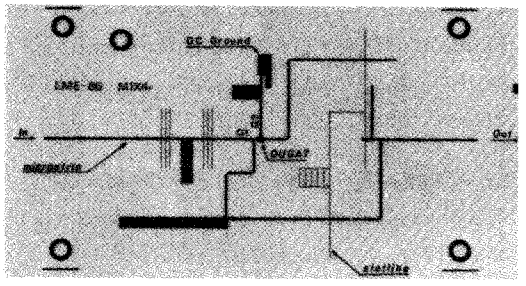


Fig. 2 - Test Circuit Photomask

## EXPERIMENTAL RESULTS

The circuit was initially adjusted to operate as an open loop frequency quadrupler for an input power level of 0 dBm at a fundamental frequency of 1.0 GHz. Figure 3 depicts the multiplication gain as a function of input power showing a maximum of 2.5 dB. The measured power performance was + 4.5 dBm with 1.5 dB associated multiplication gain and 1.9% RF-to-DC efficiency.

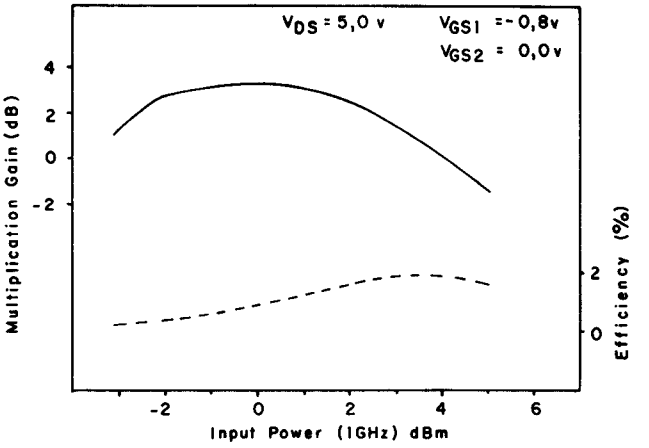


Fig. 3 - Measured Performance of Open Loop Frequency Quadrupler

In the next experiment the feedback loop was closed and part of the output harmonic was coupled to the input. The circuit then acted as a 10 mW oscillator at 4 GHz. Circuit adjustments giving stable operation were found to severely degrade the performance as a multiplier. However, this system operated as a subharmonically synchronized oscillator to 1 GHz, with a locking bandwidth less than 1 MHz.

Finally, the feedback path was adjusted to the next higher harmonic (5 GHz), since the lower one was partly blocked by the microstrip-to-slotline transition. Care was taken to introduce small adjustments on gate 1 and 2 tuning circuits to account for small feedback effects. In order to obtain stable operation a self bias resistor had to be introduced on gate 1. Figure 4 shows the multiplication gain as a function of input power, with a maximum of 9 dB. The measured power performance was + 9.8 dBm with 8.5 associated multiplication gain and 6% RF efficiency. Note that the power obtained at 4 GHz is very close to the power capability of the device.

Since the main purpose of the above experiments was to verify the multiplier operation at a specific fundamental frequency, the circuit was adjusted with a CW signal, without considering its bandwidth. A 3 dB bandwidth of less than 20 MHz at the fundamental frequency was obtained for both

multiplier circuits. This characteristic can be improved with a more complex circuit which may compromise gain and output power performances.

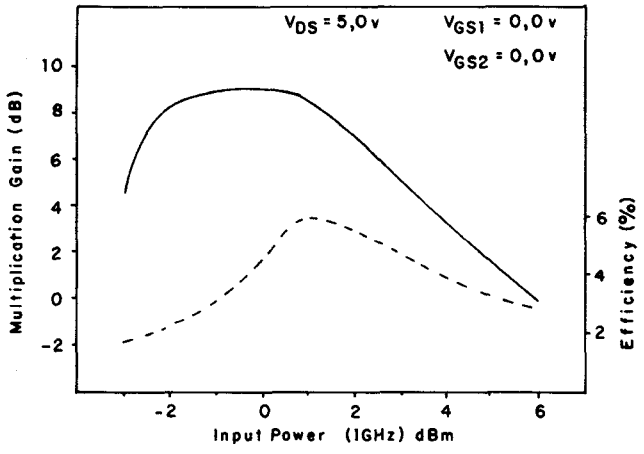


Fig. 4 - Measured Performance of Feedback Frequency Quadrupler

The top view of the prototype used in the measurements is shown in Figure 5.

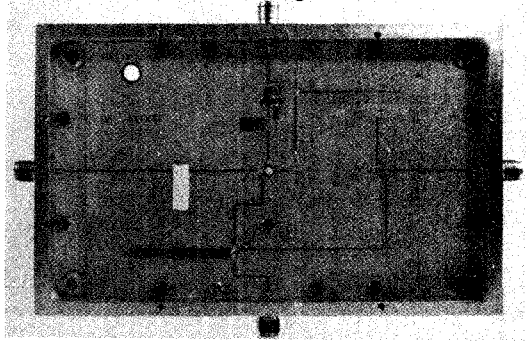

Fig. 5 - Photograph of the experimental Frequency Quadrupler

## CONCLUSIONS

The test circuit under investigation demonstrated that dual gate GaAs MESFET's give excellent performance when operating as a frequency quadrupler. The measured performance confirms the assumptions made in the operation of frequency multipliers. It also shows that a judicious feedback network has a great positive impact on the multiplication gain. The mechanisms studied in this paper apply equally to the design of frequency triplers, quintuplers,etc ... The use of positive feedback seems to be attractive for higher frequency applications,for instance in the design of millimeter wave sources, where it may compete with diode multipliers.

## ACKNOWLEDGMENTS

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