A COMPACT HIGH POWER AMPLIFIER FOR HANDY PHONES

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ABSTRACT

A compact high power amplifier module has been developed for operation within the 890 to 915 MHz band and intended for application on handy phones. The paper summarizes the design steps and the unique use of self resonating chip capacitors to increase the efficiency. The amplifier module delivers a saturated power of + 36 dBm with 55% efficiency and 36 dB gain when operating from a supply voltage of 5.8 volts.

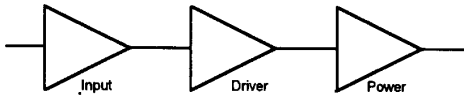
1. INTRODUCTION

At the present time there is a great interest in the design of high efficient, reliable and low-cost power amplifiers to be employed in hand held phones. The high demand for this type of component suggests the use of MMIC technology for lowering costs. However, in the case of high power operation at 900 MHz, MMIC circuits become too large which precludes this choice. Thus, the hybrid approach, employing discrete MESFETs, still provides the best combination of characteristics for obtaining a high performance power amplifier module. Examples of the hybrid approach operating at 900 MHz have recently been reported in the literature where a one stage amplifier biased at 6.2 V gave an output power of 35.5 dBm with 53% power added efficiency(1) and a two stage amplifier biased at 4.7 V gave an output power of 32.3 dBm with 65 % power added efficiency(2).

This paper describes the design of a power amplifier module aimed at high gain (36 dB), high output power (+ 36 dBm) and high efficiency (55 % @ Pout = +35 dBm) over the 890 to 915 MHz bandwidth. The amplifier circuits were designed for high volume production, so that it meets this performance without tuning for compensation of the spread of component parameters. The high efficiency was obtained with a innovative design technique for rejecting the second harmonic. The compactness was achieved by the use of miniature chip resistors and capacitors surface mounted on a low cost MIC board material.

2. MULTISTAGE AMPLIFIER

The amplifier represented in figure 1 consist of an input low level stage, a driver stage and a power output stage. The input stage is linear and operates in class A. The remaining two stages are non-linear operating in class AB for increased power added efficiency. The objectives discussed in the previous section are obtained with all devices biased at a drain bias lower than + 5.8 volts. The power budget and efficiency depicted in the figure were estimated from load pull measurements and transistor data sheets. In order to meet an overall efficiency of 55% for the amplifier module, the driver and output stage have to achieve 17% and 57% minimum efficiency respectively.



Gain (dB)	10	13	13
Efficiency(%)	10	17	57
Device	FSC11LG	FLC151XJ	FLC702XJ

Fig. 1. Amplifier Block Diagram

3. LARGE-SIGNAL TRANSISTOR CHARACTERIZATION

The device FLC702XJ employed in the output stage comprises 24 parallel cells with a total gate area of 1 X 1000 um2 and is capable of delivering an output power of 4 W at 900 MHz and 5.8 volts. The driver stage employs device FLC151XJ designed for 1 W output power at 900 MHz at the same bias. These transistors are mounted on a special package measuring 40 X 80 X 200 mils which ensures a low thermal resistance to the heat sink. The active area plus bonding wires are protected by a plastic material. The input stage employs a general purpose small signal device. A set of output devices were submitted to load pull measurements for the determination of large signal impedances, power output capability and efficiency. A typical result for the

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power added efficiency as a function of output power is depicted in figure 2. It shows a maximum efficiency of 70 % at an output power of +36 dBm with the device biased at 5.8 volts. The minimum and maximum obtained efficiencies for 12 devices were 65 and 75 % respectively.

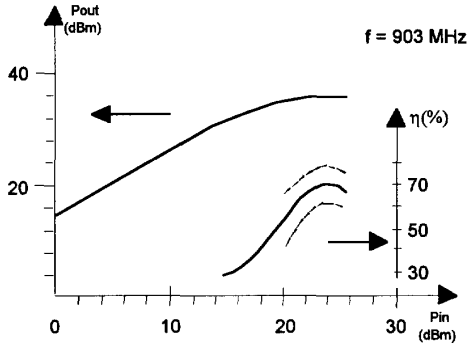

Figure 2. Performance of the high power device

4. CIRCUIT DESIGN

After consideration of available methods for designing class AB power amplifiers, it was concluded that the large signal impedances have to be accurately determined and a simple method to obtain them is through load pull measurements. However, a design based only on these results will not give information on the generated harmonics, which is essential for optimizing the RF performance. The devices employed in the driver and power stages were modeled after the Raytheon non-linear model(3) for the purpose of simulation with MicrowaveSpice. This model was chosen for its simplicity and high accuracy in representing the DC performance of power devices. Its drawbacks of overestimation of power gain and inaccuracies in the representation of large signal impedances were corrected by the load pull measurements. The corrections consisted of the introduction of losses in the model by modifying the gate resistance and by shunting the output conductance with a fixed RF resistance from drain to ground.

The RF circuit schematic for the driver and power stages is illustrated in figure 3. Only the power and driver amplifiers will be discussed in this context, since the input stage operates linearly and was designed according to conventional techniques. An output network containing two low pass cells was used for transforming 50 ohms to the optimum load resistance required by the power device. Theoretically(4), its value for maximum power is equal to 2.0 ohms. However, non-linear simulations showed that 4.0 ohms gives the best efficiency, a value in agreement with 3.7 ohms determined by load pull. The elements were determined by use of Smith Chart, where the first cell transforms from 50 ohms to 10 ohms and the second to 4 ohms.

The interstage matching requires the determination of the input impedance of the output device and the load impedance for the driver that guarantees a minimum power for driving the output stage into saturation. In this case the driver must provide at least 23 dBm linear output power which requires an ideal(4) load equal to 53 ohms. Employing this value and assuming a matched input, the driver amplifier was simulated to check its power and gain capability. A predicted maximum linear power of + 28 dBm with an associated gain of 14.5 dB was obtained. A simple low pass network was employed to transform the output device's input impedance from 2.7 ohms to 53 ohms. The input impedance of the driver stage was obtained through non-linear simulation, and was matched to 50 ohms through a high pass inductive cell.

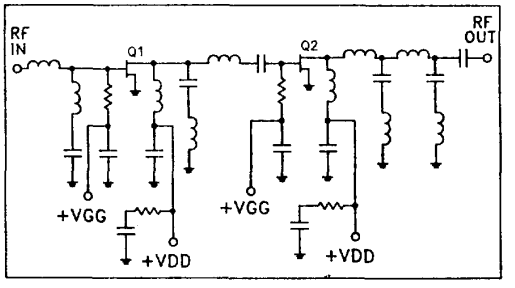

Fig 3. Schematic of the driver and power stages

The large signal simulation for the power amplifier showed a high second harmonic in the drain current coming from class AB operation. Improvements employing a quarterwave shorted stub have already been discussed elsewhere (5,6) but in the present design the board area left for matching and biasing the circuit did not allow the use of such a long line. Thus, another approach had to be used for terminating the second harmonic. Fortunately, the range of the chip capacitors used in the matching circuits presented a self resonance near 1.9 GHz which can be used for the same purpose and are easily tuned for the correct frequency. The resulting second harmonic phase at the drain port is a compromise between fundamental frequency match and second harmonic termination. The driver and output stage in conjunction with the equivalent circuit for the capacitors, gave a simulated power gain of 29 dB before entering into saturation. The output power with 4 dB gain compression is equal to + 36 dBm.

Investigation on the self resonance frequency of chip capacitors seems to be dependent on capacitor size and on tolerance of capacitance values. A series of chip capacitors were measured and showed consistent repeatability in the capacitance and in the self resonance frequency.

5. EXPERIMENTAL RESULTS

The matching circuits were constructed on a low cost high dielectric material, ER = 10, 32 mils thick, presenting an insertion loss of 0.25 dB/λ. All the matching, biasing elements and active devices are contained in a board area equal to 47 mils X 80 mils. The active devices and the boards are soldered directly to a heat sink. The circuit stability was obtained using 300 Ohms chip resistors for biasing the gate and a video filter at the drain. The chip capacitors measures 20 mils X 40 mils and presented a Q factor lower than 15. A photograph of the complete module is shown in Figure 4.

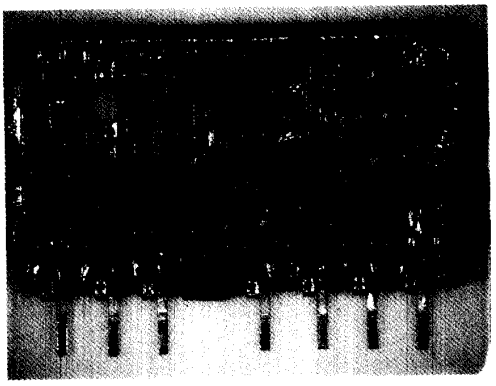

Fig 4. Photograph of the power amplifier module

The amplifier operation at mid band frequency and 5.8 volts bias resulted in a small signal gain of 40 dB and an input return loss of 12 dB. By driving the amplifier 4 dB into saturation a power output of 36.5 dBm at 57% efficiency was obtained. The measured amplifier frequency response is represented in figure 5, with the second stage bias adjusted for + 35 dBm output power. The response curve changes with power level and at maximum output power it rolls off at the high frequency end by 0.75 dB. The obtained efficiency is also represented in the figure and ranges from 55% to 59%. The non-constant efficiency was predicted in the simulations and reflect the tradeoff between second harmonic tuning and fundamental match. Another prediction made on the computer simulation showed that this result could be improved by 2% if lower loss capacitors (Q = 150) and substrates are used.

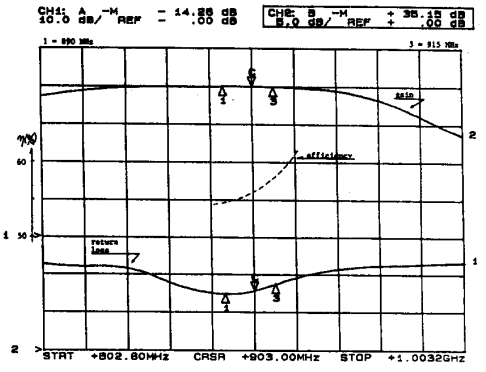

Fig 5. Frequency Response and Efficiency at Pout= + 35dBm

The amplifier performance in terms of output power and efficiency as a function of drain bias is represented in figure 6. It can be observed that with a 3.3 volt battery, the saturated power is in the order of 31.5 dBm and efficiency is better than 51%.

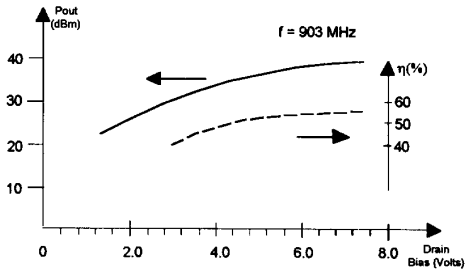

Fig 6. Power Output and Efficiency as a function of bias

Additional important results are the input return loss, which is better than 12 dB within the band and the level of harmonics at the output, which are bellow -40 dBc for second, third and fourth harmonics.

6. CONCLUSION

The design techniques and the performance of a +36 dBm saturated amplifier featuring high gain and high efficiency were described. The design approach, consisting of load-pull measurements to correct large signal modeling, proved to be successful since it was possible to optimize the matching circuits and determine adequate terminations for the second harmonic. The obtained results are considered excellent since they include the degradation introduced by circuit losses due to the substrate and to low Q capacitors. Also, it was

concluded that actual results can be well predicted by load pull and circuit simulation techniques. It can be concluded that the obtained experimental results for this amplifier are adequate for application on hand portable transceivers operating either at 3.3 or 5.8 volts bias voltages.

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