

A Balanced Resistive Mixer Avoiding an IF Balun

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Abstract — A balanced resistive mixer topology is proposed, that avoids the requirement of an external 180° IF hybrid. Instead of a balun, the IF signal is extracted once at the drain and once at the source of the balanced FETs. Thus, the IF signals can simply be combined. Operating as up- and downconverter, the fabricated MMIC mixer has a measured conversion loss of better than 10 dB over a frequency range from 29 to 39 GHz.

I. INTRODUCTION

In the next generation of millimeter wave communication equipment, complex modulation schemes like 64 QAM or COFDM will be applied to deliver the required spectrum efficiencies for the transmitted data rates [1]. Those modulation schemes require linear transceivers to maintain the required dynamic range of the transmitted and received signals. A key element in the transceiver is the mixer. In today's transceivers, a balanced diode mixer and an active mixer provide the required linearity for the transmission, but those mixers cannot achieve the linearity required for a distortionless transmission of nonlinear modulated signals. Only resistive mixers are superior to diode and active mixers in their intermodulation suppression performance [2]. Therefore, resistive mixers will play a more important role in future transmitter architectures. So far resistive mixers suffer from poor LO to RF isolation. The introduction of a balanced configuration solved the problem, but a large hybrid IF balun became necessary [3].

This paper introduces a new topology for resistive mixers in a balanced configuration which does not require an off-chip IF balun. The design steps are described, and a prototype was fabricated as a "proof of concept" for the mixer.

II. THE MIXER TOPOLOGY

The proposed mixer topology for the resistive mixer is depicted in figure 1. The basic structure is

analogous to a single-balanced resistive mixer [3]. A balun splits the LO signal into two equal amplitude but 180° out of phase signals, which are applied to the gate of each transistor. The LO signal leaking through the gate drain capacitance is cancelled at the RF input port, if the applied impedances at each device are the same. The RF signal is split into two in-phase signals and is applied to the drain of each cold FET. The resulting IF currents at the drain are 180° out of phase. Conventionally, in a single balanced resistive mixer, both IF signals are taken from the drain of the transistor. This results in the requirement of an additional IF balun to combine the signal. This solution is bulky and adds to cost.

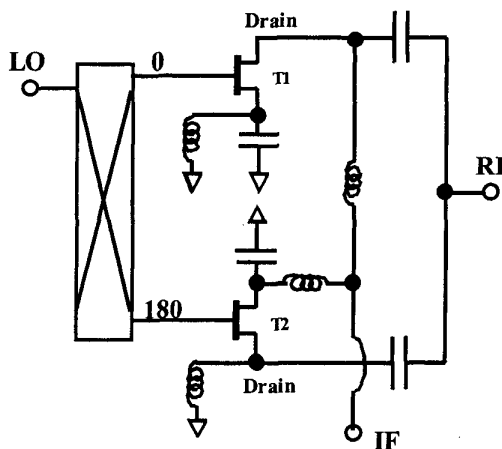


Fig. 1. Schematic block diagram of the resistive mixer topology

In the proposed topology, advantage is taken from the fact that the IF signals are in opposite phase at the drain of each transistor and a 180° phase shift exists between drain and source. Therefore, if the IF signals are taken once from the drain and once from the source of the transistors, the IF signals are in phase and can be connected together. The IF return

has to be attached vice versa at the source and drain of the FETs.

II. THE DESIGN

The design of this mixer started with the modeling of a common source “cold FET” as a function of gate bias from 0.5 to -2.0 V. The drain source resistance as a function of gate source voltage is shown in figure 2 for a $600\text{ }\mu\text{m}$ wide transistor. The device size was determined targeting a low “on” resistor to minimize conversion loss. The parasitic capacitances were extracted from small signal S-parameter measurements. The dependence of the capacitances from the gate source voltage is included in the model as user-defined equations.

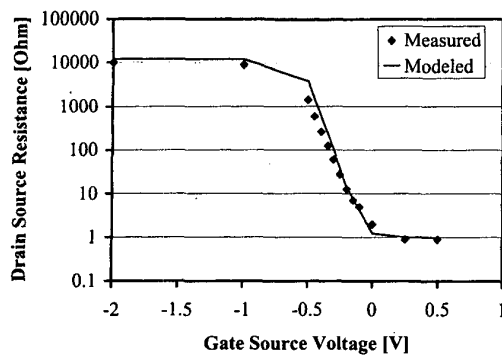


Fig. 2. Drain source resistance R_{ds} versus gate source voltage for a $600\text{ }\mu\text{m}$ cold FET

With this model, an analysis of the equivalent impedance at LO, RF and IF frequencies was carried out. The impedances were used for the determination of the matching elements.

The LO impedance was determined using the diagram depicted in figure 3, simulated in the harmonic balance simulator Agilent ADS. The device is biased at pinch-off and a large signal voltage is applied at the gate, with the source grounded and the drain terminated into $50\text{ }\Omega$. These conditions enable a high on/off R_{ds} ratio providing optimal switching characteristics for the mixer function. With the resulting gate current, the desired large signal gate impedance can be calculated.

The RF impedance was determined by applying a small signal generator at the drain and measuring the resulting current with the gate pumped by the LO

voltage. Each drain is matched to $100\text{ }\Omega$ to give a matched parallel impedance. The LO and RF equivalent impedances were matched with two stage high pass type matching networks. In the designed mixer, there was no attempt to match the IF impedance due to the required size of matching elements. The two FETs are paralleled at IF. The resulting impedance is much lower than $50\text{ }\Omega$. This impedance can be matched off chip with discrete elements and improve the conversion loss performance.

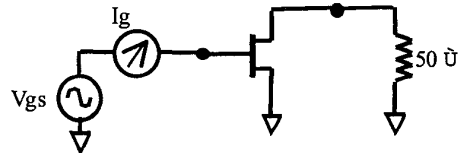


Fig. 3. Determination of the LO large signal impedance

The RF and LO matching cycle was iterative, to take account of device terminations at each port of the final circuit. It is important to maintain the circuit symmetry when joining both circuits. If an asymmetry is introduced, the 180° out-of-phase balance is destroyed, and the LO to RF leakage is degraded.

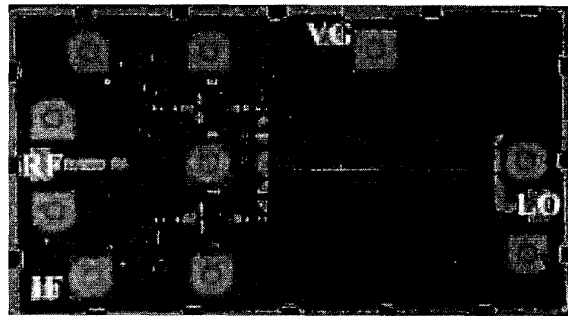


Fig. 4. Photo of the mixer: Mixer size $1 \times 1.2\text{ mm}^2$; total circuit size with Lange couplers: $2.2 \times 1.2\text{ mm}^2$

The difficulty to maintain the balance comes with the introduction of the IF access networks. On one side of the balanced configuration, the IF signal is taken from the drain of the transistor 1, on the other side from the source of transistor 2. Additionally the IF return has to be attached to the source of transistor 1 and drain of transistor 2. An easy way to implement the IF signal access is to use a low pass filter. In the chosen implementation the low pass

filter consists of a spiral series inductor with a parallel MIM capacitor to ground. For the IF return, this capacitor can be grounded with small influence in the impedances at LO frequencies. The IF signal can easily be accessed from the top of the capacitor.

The 180° phase split at the LO port was obtained by attaching two Lange couplers back to back with proper open and short terminations at the unused ports. This arrangement provided equal amplitude and phase splitting with low losses over a broad bandwidth. However, it requires a large area which is not critical for the concept verification. A photograph of the mixer is shown in figure 4. The mixer consumes a total area of $2.2 \times 1.2 \text{ mm}^2$.

The mixer was implemented in a pseudomorphic HEMT process. The gate length is equal to $0.25 \text{ }\mu\text{m}$, and the transit frequency is on the order of 30 GHz . The substrate thickness is $75 \text{ }\mu\text{m}$. The variable resistance element was implemented by a FET device measuring $12 \times 50 \text{ }\mu\text{m}^2$.

III. RESULTS

All on wafer measurements were carried out with an LO power of $+15 \text{ dBm}$. The IF frequency was set to 1 GHz in all measurements. The gate bias was selected for best conversion performance, resulting in $V_{GS} = -0.4 \text{ V}$.

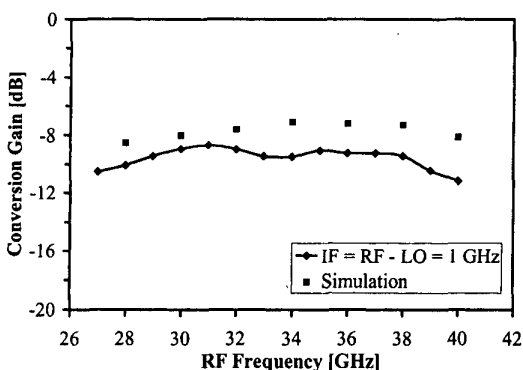


Fig. 5. Measured and simulated conversion gain as a function of RF frequency for downconverter operation

A. Downconverter Operation

The measured conversion gain as a function of RF frequency is shown in figure 5. For the frequency range of 29 to 39 GHz a conversion gain of -9 to -10 dB was measured. The simulation predicted a 1.5 dB better conversion gain.

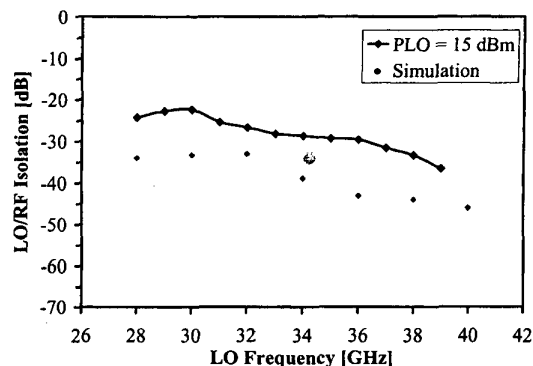


Fig. 6. LO to RF isolation versus LO frequency

The LO to RF isolation, shown in figure 6, ranges from 22 dB at the low end of the band to nearly 40 dB at the high end. The simulation predicted a 10 dB better isolation. The degradation of isolation is a result from small imbalances that may be introduced during the layout of the IF circuit.

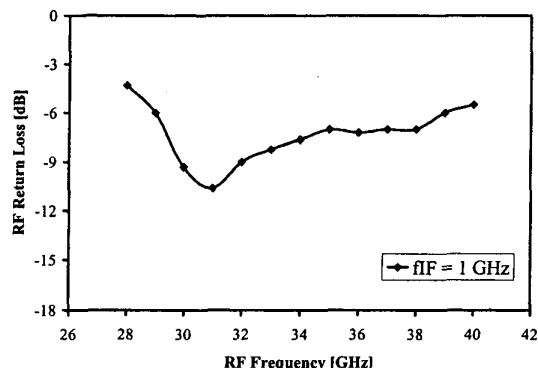


Fig. 7. Measured RF return loss versus frequency

Figure 7 shows the measured RF return loss of the mixer. The return loss is better than 10 dB at 30 GHz , degrading to 6 dB at 39 GHz . The mismatch at RF port does not depend on circuit symmetry. Instead, it represents the overall mismatch of two

paralleled impedances. If they are not similar, i. e. one drain will receive more RF power than the other, the mixer power performance is degraded. The resulting mismatch originates from inaccuracies of the "cold fet" model.

B. Upconverter Operation

Operating as an upconverter, the mixer has better than -10 dB of conversion gain from 30 to 39 GHz, as shown in figure 8. The measured conversion gain data are 2 dB better than the ones predicted by simulation. This indicates, that adjustments in the model of the cold FET have to be made, to take account of different wafers used for the model and circuit integration.

The measured compression characteristic of the mixer is shown in figure 9. The input 1 dB compression point over the band is $+10$ dBm.

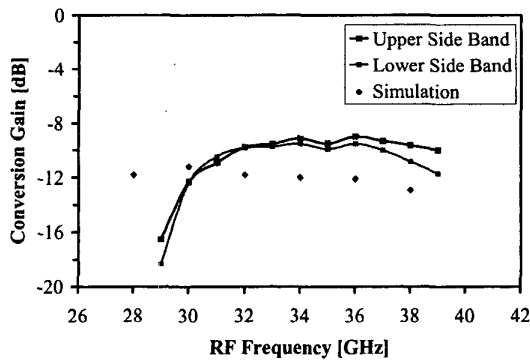


Fig. 8. Measured and simulated conversion gain

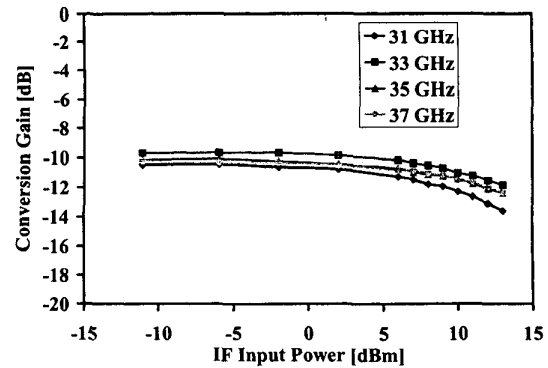


Fig. 9. Measured input power compression

IV. CONCLUSION

The operation, design and layout implementation of a balanced resistive mixer structure operating without IF balun have been discussed. In the balanced mixer, the IF signal is once taken from the drain and once from the source of the resistive FETs. Thus, the IF signals can simply be combined in phase.

To prove the concept, the mixer topology has been realized as an MMIC in p-HEMT technology. Operating as up- and downconverter, the fabricated MMIC mixer has a measured conversion loss of better than 10 dB over a frequency range from 29 to 39 GHz. Over the whole band an LO to RF isolation of better than 20 dB, ranging up to 40 dB was measured.

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