40-GHz MMICs for Optical Modulator Driver Applications

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Abstract — **This paper presents the simulated and measured performance of 50 kHz to 40 GHz distributed amplifier MMICs. The chips were fabricated in a double-doped AlGaAs/InGaAs/AlGaAs p-HEMT technology and designed using a microstrip configuration. The driver MMIC achieves 40-GHz bandwidth and provides 6.6 V_{p-p} which is ideal for Lithium Niobate optical modulator driver applications.**

I. Introduction

The use of external modulation for 10 Gbps has recently been successfully deployed for its dynamic range, high modulation speeds and minimum frequency chirp (*i.e.*, suppression of broadening of the spectral linewidth at high bit rate modulation). The availability of 40-Gbps Lithium Niobate optical modulators is contributing to the realization of OC-768 optical communication systems, pushing the envelope of today's millimeterwave, modulator IC technology. Besides the high-speed requirement, these modulators need large voltage swings in excess of 5 V_{p-p} to obtain sufficient extinction ratios at 40 Gbps. Previous publications report the use of HEMT [1] and HBT [2] devices to generate large output swings using a push-pull approach. However, there are only a limited number of solutions which demonstrate the required single-ended voltage swing and eye performance at 40 Gbps [2], [3].

This paper introduces the application of a newly developed, double-doped, AlGaAs/InGaAs/AlGaAs p-HEMT technology to the design of MMIC pre-driver and driver amplifiers for 40-Gbps modulator drivers. The design requirements include a large bandwidth from 50 kHz to 40 GHz, high gain, and low VSWR to ease chip cascading in meeting gain requirements. The output power must be large enough to generate greater than 6 V_{p-p} swing into a 50-ohm load.

II. Device Technology

The FET construction has been previously reported [3], and its main parameters are listed in Table I. The high transconductance and high cut-off frequency offered by this technology enable operation at high power with low power dissipation. Load-pull evaluation carried out at 26GHz for these devices showed each W_g = 100 µm device can provide P_{-1dB} = +12 dBm with a maximum available gain of 15 dB when biased at V_{DD} = 3.5 volts and 60% I_{DSS}.

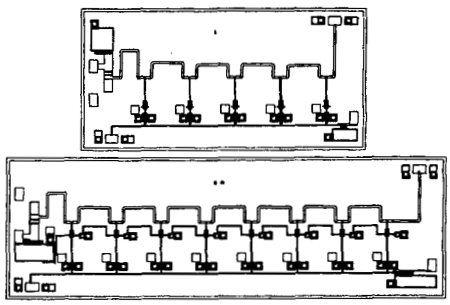

Fig. 1. Chip layouts for the pre-driver and driver MMICs. The chips are 1.3 x 2.6 mm^2 and 1.3 x 4.1 mm^2, respectively.

TABLE I
SUMMARY OF DEVICE PARAMETERS

$g_{m,max}$ = 525 mS/mm	L_g = 0.15 µm
V_{th} = -0.9 volts	f_T = 90 GHz
V_{gdo} = 7 volts	f_{max} = 130 GHz
I_{DSS} = 310 mA/mm	R_{th} = 165 °C/W

For these devices, both small-signal and large-signal models were extracted and used in the simulations that follow. The small-signal models are based upon a single-finger device model that is then connected with transmission line elements to form the top-level models of the common-source and common-gate devices. The large-signal model is based upon an EEHEMT model that was generated by using IC-CAP modeling software.

III. Circuit Design

The objectives for the circuit design are to achieve a DC-to-40-GHz bandwidth and an output voltage swing of 6 V_{p-p} in a 50-ohm system. The reference frequency

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for the power calculation is 26 GHz. For this case, the corresponding CW output power level is approximately equal +19.5 dBm.

In order to construct an amplifier to meet the proposed requirements, it was decided to employ a distributed amplifier approach. This topology is known for providing high output power and good input and output return losses for a wide operating band. Within the distributed amplifier, a cascode configuration for each gain cell was employed. This approach offers high isolation between the input and output ports due to reduced feedback capacitance and an up to 3-dB higher output power obtained from lower breakdown voltage devices, compared to a common-source configuration. In addition, the output impedance becomes very high, favoring insertion in a distributed design. Another interesting property of the cascode cell is the phase compensation between common-source and common-gate devices that results in an amplifier with more linear phase characteristics at high power levels.

The number of gain cells required can be estimated from the measured common-source load pull data. This value can be scaled by introducing the increase in power due to the cascode configuration, considering circuit losses, and providing a margin based upon the fact that each cell does not contribute the same power. It was found that 8 cascode cells using 80 μm devices are required to deliver the P_{-1dB} power at 26 GHz for the driver stage MMIC shown in Fig. 1, where the chip is 1.3 x 4.1 mm^2. The pre-driver stage MMIC (also Fig. 1) consists of a 5-cell distributed cascode amplifier, using 100 μm devices, to provide a lower gain, lower power compliment to the driver chip. The pre-driver chip area is 1.3 x 2.6 mm^2. Final output power was confirmed through non-linear simulation for both chips.

Each distributed amplifier was designed following a conventional approach. High impedance lines and device capacitances were used to form the distributed transmission lines. Because line losses increase at high frequencies, it is difficult to obtain the desired 40-GHz bandwidth with the present devices. Therefore, it was decided to compensate the losses with negative resistance generated by an appropriate gate circuit on the common-gate device, in the manner described previously in reference [4]. The circuits were then optimized using the simulator. With this technique, it was possible to obtain gain at 40 GHz with unconditional stability of the amplifier.

The gate and drain termination have a low-frequency cut-off of about 1.5 GHz due to the value of capacitance that can be built on the chip to decouple the bias supply. Therefore, the grounding of the internal gate and drain loads must be implemented off-chip. Using the same high frequency termination at low frequencies would also result in a high peak gain in the range of kHz to MHz due to differences in the device low-frequency gain. As a result, different terminations must be used externally to level off the gain at these low frequencies. This approach raises a particular problem because the self-resonance of off-chip inductors, capacitors and bond inductances are amplified by the high device gain at low frequencies and impact gain flatness. The solution was to simulate a four-port S-parameter network for the MMIC chip. Adding two ports, with reference planes at the center of the gate and drain bias terminal bonding pads, to the RF input and output ports defined the four ports for the distributed amplifier. The resulting network was then optimized with the external terminations using equivalent circuits for each chip element in the simulations.

These bypass circuits can also be used for a different purpose. There is an on-chip series resistor between the bond pad for the bypass circuitry for both the gate and the drain lines. As a result, external bias can be applied to the gate and/or drain through its respective bypass circuit. The result provides a means to apply drain bias without the requirement of a high-frequency bias coil external to the chip. The use of this approach is limited because the series on-chip resistor in the drain bias path has a maximum current limitation, and there can be a significant voltage drop across the resistor. This limitation may not be an issue for pre-driver stages with low output power requirements.

IV. Results

In order to perform small-signal and large-signal MMIC evaluation, each chip was mounted on a carrier with AuSn solder. External bypass components were wire-bonded to the gate and drain terminations to control the low-frequency response. The external bypass circuit at the gate consists of two wire bonds to a shunt 39 pF chip capacitor which is connected in parallel with a series 10 ohm resistor and 0.1 μF surface mount capacitor. The drain bypass circuit consists of two wire bonds connected to a shunt 220 pF chip capacitor in parallel with a shunt 0.1 μF surface mount capacitor. These bypass circuits are assembled in a manner similar to that described in [5]. Each MMIC was then measured using GSG wafer probes at the RF input and RF output pads, where the gate and drain biases were applied through bias tees.

Fig. 2 shows the measured and simulated s-parameter results for the driver stage MMIC (V_{DD} = 7 V and I_{DD} = 180 mA). The simulated data was generated during reverse engineering by placing an updated small-signal model in the original circuit design. The measured results show a positive 3-dB gain slope, where the gain

varies from 14.3 to 17.3 dB over the range of frequencies up to 40 GHz. The positive gain slope was designed to offer small-signal gain equalization to compensate any high frequency losses experienced in application. The pre-driver chip provides 9.2 to 12.2 dB small-signal gain over the band from 50 kHz to 43 GHz (V_{DD} = 4 V, I_{DD} = 118 mA). Both chips have been designed to provide a very smooth response that optimizes phase linearity for better jitter performance in digital applications.

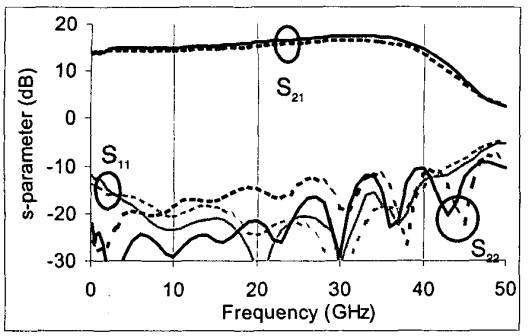

Fig. 2. Measured (—) and simulated (---) small-signal s-parameter results for the driver MMIC chip (V_{DD} = 7 V and I_{DD} = 180 mA)

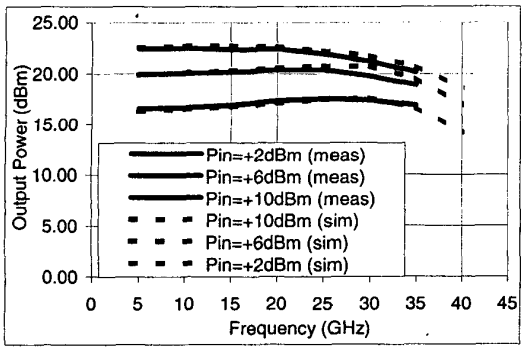

Fig. 3. Measured (—) and simulated (---) output power as a function of input power and frequency for the driver MMIC (V_{DD} = 7 V and I_{DD} = 180 mA)

Fig. 3 shows the measured and simulated MMIC output power dependence upon frequency and input power for the driver stage (V_{DD} = 7 V and I_{DD} = 180 mA). Both the measured and simulated data show that the positive gain slope at small-signal power levels is eliminated as the amplifier enters compression. In this plot, the simulation data has been normalized to account for the process variation of I_{DSS} relative to the nominal large-signal model. The large-signal bandwidth is very important because its flatness is related to the eye diagram profile when the amplifier is operated in compression.

Fig. 4 shows the measured dependence of 20-GHz CW output power compression upon drain voltage for the driver MMIC. Since this drain voltage can control the gain compression, it can also be used to control the output power of the MMIC. The plot shows that the output power P_{-3dB} can reach as high as +21.5 dBm for the driver MMIC, and P_{-3dB} = +22.5 dBm was achieved for V_{DD} = 7 V, I_{DD} = 180 mA. The pre-driver chip has a similar behavior and a P_{-3dB} power up to +19 dBm.

In order to perform time domain evaluation at 40 Gbps, 50-ohm alumina substrates were mounted on the carriers. These 0.005" thick substrates were double wire-bonded to the RF input and RF output pads of the MMICs. The carrier was then placed on a fixture with high frequency launchers contacting the substrates. Each launcher has a frequency dependent loss of approximately 0.5 dB at 20 GHz.

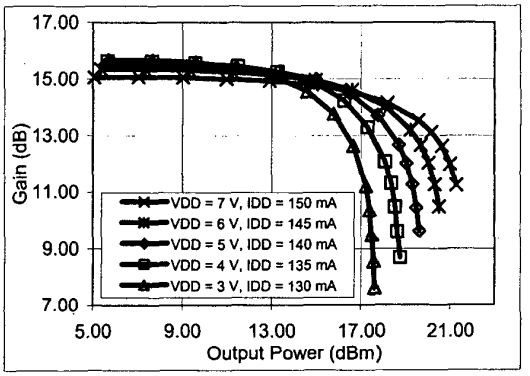

Fig. 4. Measured gain compression as a function of output power and bias for the driver MMIC

Fig. 5 shows the measured output eye diagram of the pre-driver and driver stage MMICs in linear operation at 40 Gbps. The 2^{31}-1 pseudo-random bit sequence input signal for both chips has jitter = 1.82 ps and eye S/N = 7.50. The pre-driver output signal shows a jitter of 1.89 ps, eye S/N = 5.24, and the eye amplitude gain is 11.5 dB. The driver output signal shows a jitter of 1.82 ps, eye S/N = 7.09, and the eye amplitude gain is 15.2 dB.

As the input signal is increased in magnitude, the MMIC amplifiers enter compression. This case is shown in Fig. 6 for the pre-driver and driver stages. The input signal has jitter = 1.81 ps and eye S/N of 8.30. Compressing the output stage provides output jitter of 2.12 ps and significant eye S/N improvement to 11.83. The input signal is 1.9 V_{p-p}, so the compressed eye amplitude gain is 10.8 dB for the output eye amplitude of 6.6 V_{p-p}. Similarly, the pre-driver output signal

provides output jitter of 2.13 ps and eye S/N 11.14 where its eye amplitude of 4.2 V_{p-p} corresponds to a compressed gain of 6.9 dB.

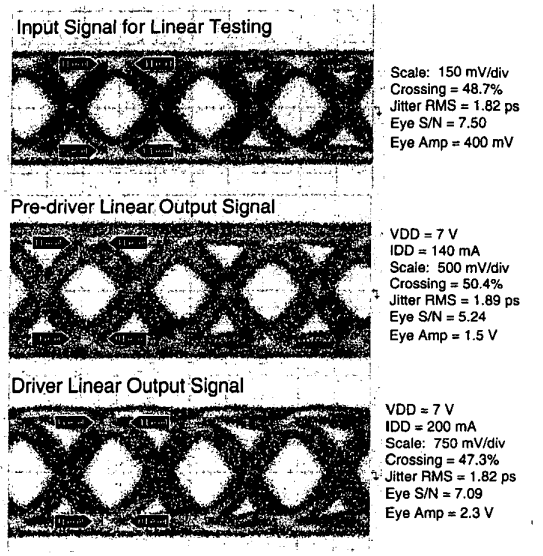

Fig. 5. Measured input and linear mode output 40-Gbps eye diagram results for the pre-driver and driver MMICs

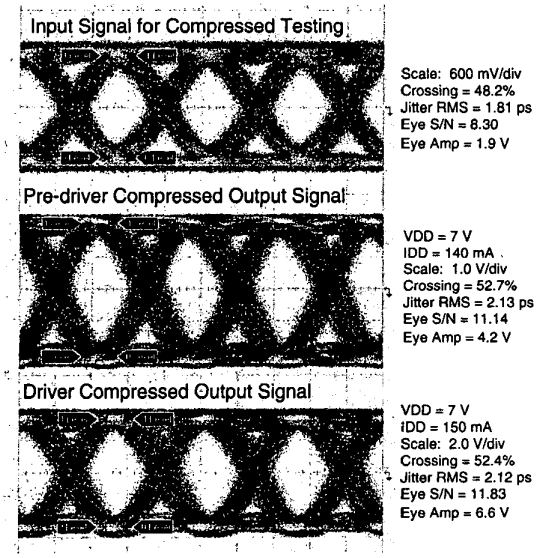

Fig. 6. Measured input and compressed mode output 40-Gbps eye diagram results for the pre-driver and driver MMICs

In the linear mode of operation, the small signal gain of the amplifier dictates the time domain performance. For 40 Gbps applications, the amplifier should provide a flat frequency response with good phase linearity to 32 GHz and preferably beyond. If this performance is possible, the eye S/N will not significantly degrade and jitter performance will be good. Both the pre-driver and driver presented here, show minimal jitter degradation in the linear mode, but the driver eye S/N is clearly better for the driver circuit. This is most likely due to the fact that the positive gain slope of the driver MMIC compensates the high frequency losses of the test fixture.

In the compressed mode of operation, the amplitude of the eye is larger and the bands at the top and bottom of the eye become thinner as both amplifiers compress. This contributes to the improved eye S/N performance relative to the linear operation.

The measured jitter is also degraded for compressed operation. Circuit simulations show that the phase variation over input power is minimal. We believe that, as the devices are compressed, the input noise and jitter is up-converted to the output similar to the means in which any nonlinear element translates injected signals. Another likely cause may be the internal self-bias protection of the MMIC that enters operation at higher input signals to prevent excessive device gate currents.

V. Conclusion

This paper demonstrated distributed amplifier MMICs for LN modulator driver applications. Using microstrip technology in a newly developed, double-doped, AlGaAs/InGaAs/AlGaAs p-HEMT process, the designs provided approximately 40-GHz bandwidth with large output eye amplitudes of up to 6.6 V_{p-p} at 40 Gbps. The results presented also show the effect of linear and compressed operation upon the eye diagram for each chip.

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