A Highly Integrated Ka- band MMIC Quadrupler

Keigo Kamozaki, Thomas A. Bos and Edmar Camargo

Fujitsu Compound Semiconductor, Inc., 2355 Zanker Road, San Jose, CA 95131-1138 USA

Abstract — **A highly integrated monolithic microwave integrated circuit (MMIC) frequency quadrupler was realized in a 0.25μm pHEMT technology on GaAs. The quadrupler consists of two types of doublers and two buffer amplifiers. An active balun and a planar balun using an asymmetric coupled line were used for each doubler to reduce the chip size and to achieve higher gain and output power in comparison with conventional quadruplers. Realized on a chip size of 1.2x2.3 mm^2, the quadrupler delivered an output power of 19.4 dBm for an input power of 5 dBm over an output frequency range of 36 – 40 GHz. The maximum conversion gain of 16.4 dB was measured for an input power of 2dBm. In saturation, the fundamental is suppressed by 58 dB and the third harmonic by 66 dB.**

Index Terms — **Converters, analog multipliers, MMICs, MMIC amplifiers, FETs, FET integrated circuits.**

I. Introduction

Excellent phase noise and low cost local oscillator frequency sources will be crucial for the development of Ka-band high-bit rate wireless link systems such as point-to-point radios or point-to-multipoint radios. The signal generation can be realized either directly by a low phase noise Ka-band oscillator or by multiplication of a low frequency oscillator. The multiplication approach offers the advantage that the oscillator can be fabricated in low cost, low phase noise, silicon bipolar technology. A compact quadrupler is required if a local oscillator frequency of 9 GHz is chosen. Some published MMIC quadruplers [1][3] still require further chip shrinkage and an improvement in the output power performance.

In this paper, the design and measured results of a highly integrated quadrupler is presented. Due to the chosen configuration, the quadrupler achieves high conversion gain and high output power level with, at the same time, excellent suppression of undesired harmonics.

II. Circuit Design

For the chip fabrication, Fujitsu's double δ-doped AlGaAs/InGaAs/AlGaAs pHEMT process technology with 0.25-um T-gates was used. The transistor has a transconductance of 300 mS/mm and a maximum frequency of oscillation of 85 GHz biased at Vds=6V 70% Idss. For the simulation of the doublers and buffer amplifiers, an EEHEMT model and a small signal model were extracted.

The block diagram and chip photograph are shown in Figures 1 and 2. The chosen quadrupler configuration consists of a 9-18-GHz doubler, an 18-GHz buffer amplifier, a second doubler and a 36-GHz output amplifier. This configuration has major advantages over a single quadrupler approach. In the single quadrupler approach, the fourth harmonic is directly extracted from a rectified half-wave sinusoid. Thus, the conversion efficiency is low. The output power of the quadrupler has to be amplified by a cascade of several output amplifiers, which results in a large chip size and DC power consumption. In the proposed configuration, the doublers have higher output power levels and require only a few amplifier stages to provide the required output power level. For minimization, different types of doublers were integrated. As a further advantage, the 18-GHz buffer amplifier improves the rejection of input signal and also helps stability. The 18-36-GHz doubler is isolated from load by the 36-GHz output amplifier.

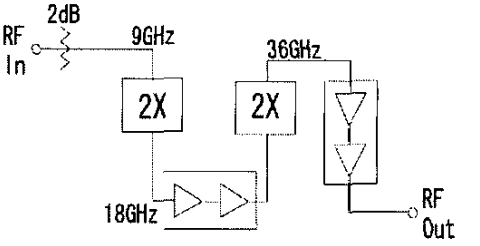

Fig. 1. Block diagram of the MMIC quadrupler

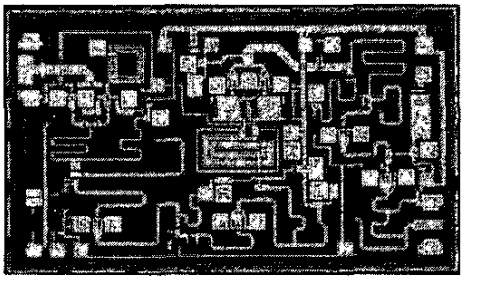

Fig. 2. Chip Photograph of the MMIC quadrupler. The chip size is 1.2mm x 2.3 mm^2.

0-7803-8331-1/04/$20.00 © 2004 IEEE

A. 9-18-GHz doubler

Figure 3 shows the schematic diagram of the 9-18-GHz doubler. The size critical balun has to be carefully designed to achieve minimum chip size. Therefore the active- balanced doubler topology is used instead of passive balun and transistor combination. In the doubler, a simple combination of common-gate-FET (CGF) and common-source-FET (CSF) with two 100- μm gate width transistors provides the required 180-degree phase difference for the cancellation of the fundamental. This active balun has the advantage of small size at low frequencies. But, its stability has to be investigated in contrast to a passive balun. This active doubler has to be unconditionally stable for all input impedance attached.

The stability of this balun was investigated in two ways. First, a potential loop oscillation, which can be caused by 180-degree phase differences within the loop branches, was checked with a method published in [4]. Second, the in phase stability within the circuit was confirmed by simulating the K-factor of circuit. To avoid negative resistances at gate and drain of the common-gate-FET, a series resistance Rcg, which is shown in the figure 3, is added to gate. This reduces the gain, but it improves stability by decreasing the loop gain at the same time. In addition, the series resistors Rdl are added in both drain connectors to decrease the loop gain. Consequently the doubler showed unconditional stability during the in-phase and out-of-phase stability simulation. However, those minimum resistor values should be carefully chosen with margins for temperature and process variations, because conversion gain is degraded by the increased stability.

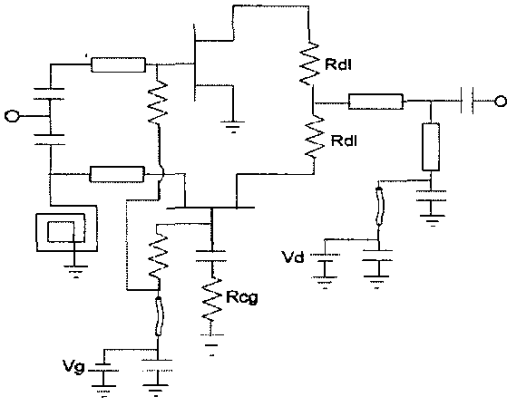

Fig. 3 Schematic diagram of the 9-18-GHz doubler

The doubler has a short stub and a series transmission line for an output impedance adjustment at the connection of two drains. These elements provide a short for the fundamental and additional match for the second harmonic. The bias point was chosen at Vg=0V to obtain high fundamental suppression and second harmonic, as the simulation showed.

B. 18- GHz buffer amplifier

Figure 4 shows the schematic diagram of the 18-GHz buffer amplifier. For the rejection of harmonics and higher gain, the amplifier was designed narrow band with a 200 μm transistor in the first stage and a 300 μm in the second stage. At the same time the amplifier isolates the first and the second doubler and pumps enough input power into second doubler. It was designed for single bias supply operation. Each stage has a parallel resistor with capacitor network to reduce low frequency gain and improving stability at low frequencies. In the design, the resistive feedback stabilization was avoided to achieve maximum isolation.

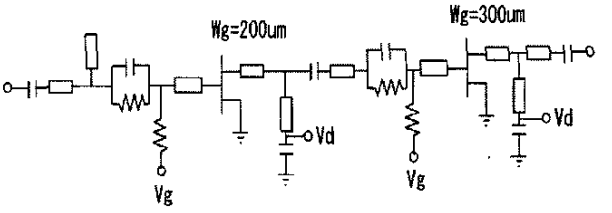

Fig. 4 Schematic diagram of the 18- GHz buffer amplifier

C. 18-36- GHz doubler

(a) Balun design

For this frequency, the active balun configuration, as used in the 9-18-GHz doubler, has no advantage in terms of size. Furthermore, the active balun configuration balun has less output power capability. Therefore a unique planar balun was designed. The photograph and simplified schematic diagram of the balun are shown in Figure 5. The layout size of the balun is comparable with the active 9-18-GHz doubler.

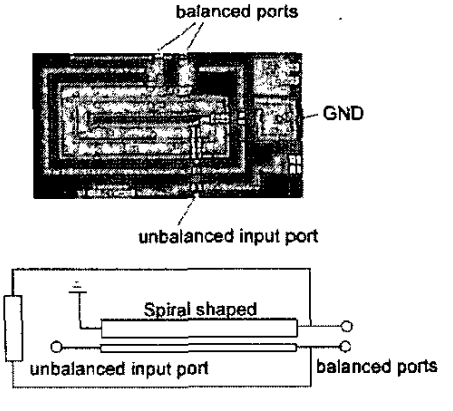

Fig. 5. Photograph of the balun and simplified schematic of the 18-GHz balun

The planar balun was designed to provide equal amplitude and differential phase at the balanced ports. The 180- degree hybrid consists of coupled lines and an additional transmission line. A single coupled line section is wrapped into a spiral to form a simple compact balun. The transmission line, which connects both balanced ports, equalizes the amplitude level of both ports. However, the transmission line limits the bandwidth, because of its fine coupling tuning. Asymmetric coupled lines were employed instead of symmetric coupled lines to obtain tight coupling between the ports. This improves the relative bandwidth by more than 50% compared to a conventional planar balun [2]. The structure has a smaller layout size and comparable performance in comparison with a planar marchand balun [5]. The coupled line length and strip widths were designed and optimized using commercially available 2D EM simulation software.

(b) Doubler design

Figure 6 shows a schematic diagram of 18-36-GHz doubler. The doubler configuration is the same as a single balanced resistive mixer [6]. It consists of the previously described balun, a pair of transistors, and an output-matching network. The output-matching network has a transmission line and a shorted stub, which minimizes fundamental and matches the second harmonic. 200- μm wide transistors are used to achieve high output power. The bias point was selected near pinch-off in order to generate a drain current that is rich of the second harmonic. During stability simulation, loop gain was calculated for high input power levels. For small input power levels, the transistors operate near pinch-off and have no oscillation possibility due to their low gain. However, drain current flows and the operating point will be shifted if high RF input power is pumped. As a result, the transistor will have higher transconductance. The resistors between the gates are used to supply the bias voltage and to avoid loop oscillation. The parallel resistor with capacitor network in series with the transistor gate improves the stability of the circuit.

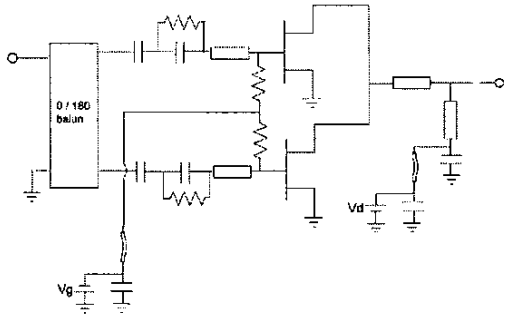

Fig. 6. Schematic diagram of the 18-36-GHz doubler

D. 36-GHz buffer amplifier

The 36-GHz amplifier is designed for narrow band operation as output amplifier. The circuit topology is the similar to the 18-GHz buffer amplifier. The transistors of the two stages have device sizes of 200 μm and 300 μm. The amplifier operates from a single bias supply voltage. This amplifier increases the output power of the 18-36-GHz doubler and isolates the second doubler from the load.

III. Measured MMIC Performance

The quadrupler and additional functional blocks were tested on-wafer using GSG probes based on a scalar power setup. The functional blocks were built to measure their performance individually. The measurements were done with a drain voltage of 6V.

Figure 7 shows the measured output power of the individually built 9-18-GHz doubler for an input of 10 dBm. The doubler achieves a conversion loss of 5.5 dB and delivers 4.5dBm output power at the second harmonic. The fundamental suppression is more than 23 dBc at 10.5 GHz input frequency.

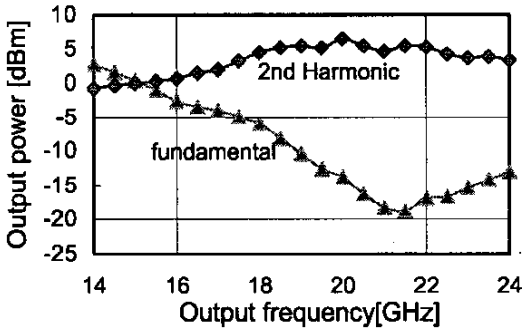

Fig. 7. Output power of the 9-18-GHz doubler at an input power of 10dBm

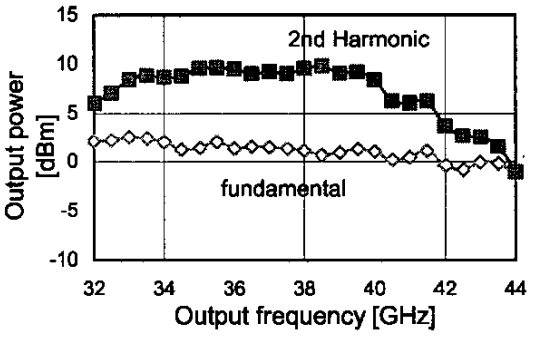

Fig. 8. Output power of the 18-36-GHz doubler at an input power of 11dBm

Figure 8 shows the output power of the 18-36-GHz doubler for an input of 11 dBm. A second harmonic output power of 9.5 dBm and conversion loss of 1.5dB were measured at 18GHz input signal. The balun has an insertion loss of 1.9 dB from 16 to 34 GHz. The phase imbalance between the balanced ports was less than 8 degree over the 18-38 GHz range. The return loss of the unbalanced port is less than -10dB from 18 to 28 GHz. The 36-GHz buffer amplifier has a small signal gain of 12dB and delivers a saturated power of 20.1 dBm.

Figure 9 shows the measured output power of the quadrupler as a function of frequency for an input power of 4.5 dBm. The quadrupler delivers 19.4 dBm at 38 GHz. The suppression of 9- GHz fundamental input and 27-GHz third harmonic signal are 58 dBc and 66 dBc, respectively. The suppression of second harmonics is more than 30dBc over 36 – 40 GHz. The flatness of output power of the quadrupler is 0.36 dBpp from 36 GHz to 40 GHz band.

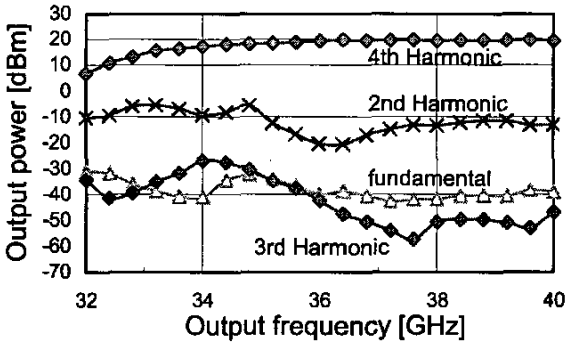

Fig. 9. Output power of the quadrupler as a function of frequency at an input power of 4.5 dBm

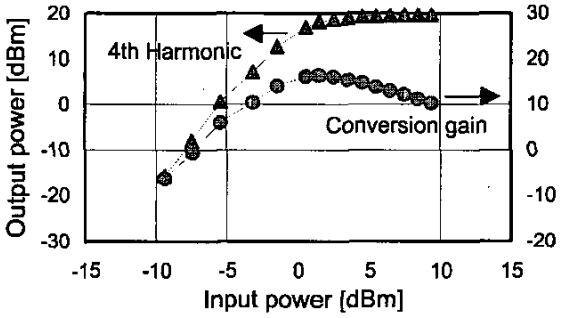

Fig. 10. Output power and conversion gain of the quadrupler at the output frequency of 38 GHz

Figure 10 shows the output power and conversion gain as a function of the input power at an output frequency of 38GHz. The quadrupler has a saturated fourth harmonic output power of 19.7 dBm for a 7.5 dBm input signal. The saturated output power was limited by the saturation of the 36-GHz buffer amplifier. For 2 dBm input power, the quadrupler has its maximum conversion gain of 16.5 dB. The total quiescent current of the quadrupler is 266 mA. Its power added efficiency is 6% and higher than a single quadrupler approach. In addition, its efficiency is better than published quadruplers and doublers [1][7-9].

IV. Conclusion

In this publication the design of a small size MMIC quadrupler operating at Ka-band is explained and measured results show a remarkable performance. The doubler designed with an active balun and a passive planar balun are realized with two buffer amplifiers for isolation and harmonic rejection. The advantages of the chosen configuration are discussed in terms of stability and layout size. With a chip size of 1.2 x 2.3 mm^2, the quadrupler delivers an output power of 19.4 dBm in saturation over the 36-40 GHz band. It achieves 16.4 dB conversion gain and a minimum fundamental, second and third harmonic suppression of 58, 30 and 66 dBc, respectively.

Acknowledgement

The authors wish to acknowledge Ryan Pham for his measurement support.

References

[1] T. Tokumitsu, "K- Band and Millimeter- Wave MMICs for Emerging Commercial Wireless Applications", IEEE Trans. on Microwave Theory and Techniques, VOL. 49, No 11, November 2001, pp. 2066 - 2072

[2] R. S. Virk et al, " A Ku-Band Frequency Converter using 0.25 μm PHEMT Technology", IEEE MTT-S International Microwave Symposium, 2000, pp. 639 - 642

[3] Y. Campos-Roca et al, "Coplanar pHEMT MMIC Frequency Multipliers for 76-GHz Automotive Radar", IEEE MWGL, VOL 9, NO. 6, June 1999, pp. 242 -244

[4] T. Takagi et al, " Analysis of High Power FET Amplifier Instability due to fo/2 Loop Oscillation", IEEE 1994 Asian-Pacific Microwave Conference Proceedings, 1994, pp. 571-574

[5] M. Shimozawa, " A Parallel Connected Marchand Balun Using Spiral Shaped Equal Length Coupled Lines", IEEE MTT-S International Microwave Symposium, 1999, pp. 1733 - 1736

[6] K. Kamozaki et al, "50 – 100GHz Octave band MMIC Mixers", 1997 RFIC symposium, 1997, pp. 95 - 98

[7] H. Zirath et al," Analog MMICs for Millimeter-Wave Applications Based on a Commercial 0.14-μm pHEMT Technology", IEEE Trans. on Microwave Theory and Techniques, VOL. 49, No 11, November 2001, pp. 2086 - 2092

[8] C. Fager et al," High Output Power, Broadband 28-56 GHz MMIC Frequency doubler", IEEE MTT-S International Microwave Symposium, 2000, pp. 1589 - 1591

[9] Y. Shizuki," A 12/24 GHz Frequency Doubler MMIC Using Resistive Series Feedback Circuit", IEEE MTT-S International Microwave Symposium, 1999, pp. 307 - 310