28V High-Power GaAs FET Large-Signal Modeling Achieves Power and Linearity Prediction

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***Abstract* — This paper presents a large-signal model developed for a packaged 28V GaAs FET power device, suitable for high-power Base Station Applications. The model is capable of predicting external load and source impedances that enable the device to provide desired power and linearity (IM3 and IM5) performance. It also takes into account the device temperature difference between the unit-cell transistor and the whole multi-cell device. Therefore, design cycle of high power PA modules are shortened and so is the development of internally matched devices for other frequencies. The paper shows an application example for a P_{1dB} of 80W.**

I. INTRODUCTION

Until recently, the market for high voltage transistors, targeted to L-band Base Station Applications, was dominated by LDMOS technologies [1,2]. Now an alternative showing higher power and linearity performance is available with high breakdown voltage GaAs FET technology. These technologies are suitable for 28V operation and deliver power in the range of 80 to 300 W, with good linearity performance. The tradeoff of the design parameters can be more effective if a large signal model is used for the active device. Additionally, a model is key in reducing the long design cycle usually associated with internally matched prototyping and is very useful for the PA development and system analysis.

The behavioral modeling is the most used to represent high-power devices [3], where the AM/AM and AM/PM characteristics are predicted for a single specific source and load impedance set (usually 50Ω terminations) and specific bias. Such model is useful in system simulations where specification is well defined but not useful for the design and tuning of internally matched PA devices. In such a case, the conventional equivalent circuit-based models are still more suitable for high-power PA design.

In this paper we report the modeling work for high-voltage/high-power packaged device by presenting an equivalent circuit-based large-signal model suitable for 28V operation. In Section II, the Fujitsu new 28V GaAs FET technology used in this work is briefly introduced. Section III explains the modeling approach and steps followed to create the model. Section IV explains the unit-cell intrinsic model adjustment to take into account the temperature effect on the multi-cell device. The model validation results for power and linearity performance are shown in Section V.

II. 28V GaAs TECHNOLOGY

This work has been done using the new Fujitsu 28V GaAs FET technology, currently in production, dedicated for high-power L-band base station market. This process technology has a typical breakdown voltage of 80V allowing a flexible operation at 28V drain voltage. It has a gate length of 0.6um, Idss = 38mA/mm, Gm=149mS/mm.

The cross section schematic of the FET structure is shown in Figure 1. Higher breakdown voltage is achieved by overhanging the gate electrode and optimizing the gate-to-drain distance.

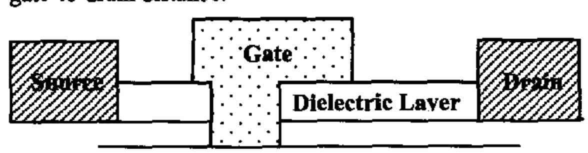

Figure 1 *Schematic cross-sectional view of the developed GaAs FET.*

This technology exhibits an output power density of 1.0W/mm with an associated linear gain of 16.5dB at 28V operation in the L-band frequency range [6].

III. MODELING APPROACH

In the initial phase of this work, both the Angelov [5] and the EEHEMT1 [7] large signal models were used to predict inter-modulation products of a unit cell device. Both models provided very similar results and we decided for the EEHEMT1 just for our own convenience; its extraction is completely automated in the parameter extractor IC-CAP by Agilent [8].

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The multi-cell 80W large-signal model has been developed in three steps. 1) Unit cell Modeling through: DC-IV measurements, S-parameters function of bias and load pull for power and inter-modulation. This modeling step was performed on wafer probe station. 2) Multi-cell (80W in this case) modeling: scaling of unit-cell model associated with the internal pre-matching circuit plus the package feed-thru equivalent-circuit. 3) Conventionally, validation of non-linear model is performed by the use of harmonic power data (f0, 2f0 and 3f0) [4,5], which may not be valid in the case of multi-tone signals where the effect of base-band frequency impedance becomes important. In this paper this issue is addressed by making Inter-modulation evaluations of packaged device to fine tune the non-linear model parameters. Additionally, the model is corrected for errors of scaling, package parasitics and temperature effects. The evaluation was carried out on a custom ICM (*Inter-Continental Microwave*) test fixture. This fixture has a gold plated copper heat sink to maximize the heat transfer from the device due to high DC power dissipation.

Figure 2 shows an overall schematic of the multi-cell large-signal model developed. This Figure shows input and output blocks of proprietary internal pre-matching circuits and the package feed-thru model. Figure 3 shows the unit-cell EEHEMT1 model [7] used for the active part.

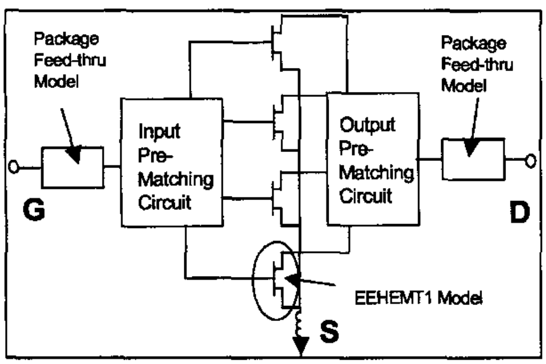

Figure 2: *Overall Schematic of the Internally-pre-matched 80W device Model.*

The modeling procedure was applied to a specific sample for a device presenting a typical I_{DSS} current. In general, models are normalized to the measured current so that a specific sample can have its parameters corrected for a different I_{DSS}. In this way, unavoidable process variations can be accounted for, with reasonable accuracy, with a single model.

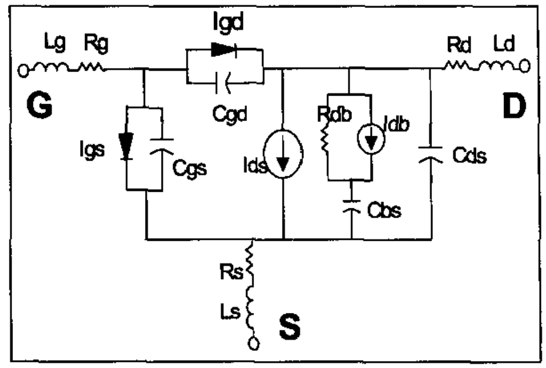

Figure 3: *EEHEMT1 Equivalent-Circuit Non-Linear Model of the unit cell transistor [7].*

IV. TEMPERATURE SCALING

During DC characterization of both unit-cell and multi-cell devices, it was found that, due to the difference in the devices temperature, the threshold voltage, V_{th}, and the DC trans-conductance, Gm, do not scale well. Figure 4 shows the DC-IV characteristics predicted by the scaled original unit-cell model compared to the actual multi-cell (80W) measurement. It is shown a large discrepancy between them. To better fit the DC-IV characteristics of the multi-cell device, the model's temperature coefficients, available in the EEHEMT1 model, were properly adjusted.

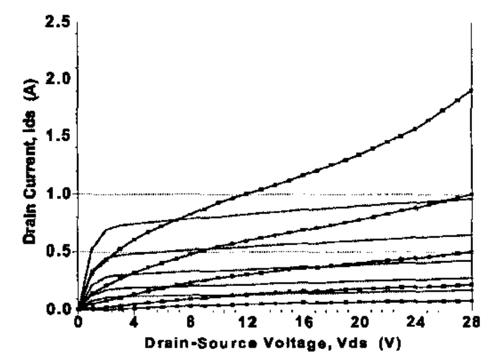

Figure 4: Measured vs. simulated DC-IV Characteristics of the 80W device using the scaled original unit-cell model; __Model, _x_x_Measurement.

The DC-IV data of the adjusted model compared with the measured results for the multi-cell device is shown in figure 5.

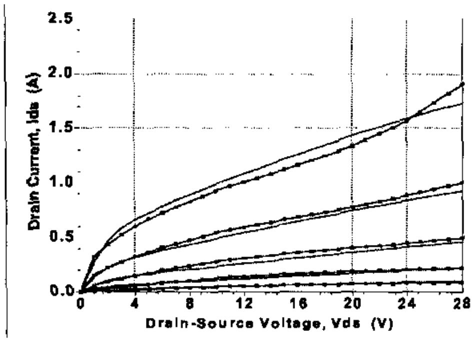

Figure 5: *Measured vs. simulated DC-IV Characteristics of the 80W device after adjustment of the model's parameter temperature coefficients; __Model, _x_x_Measurement*

V. POWER and LINEARITY PREDICTION RESULTS

To validate the multi-cell large-signal model, single-tone and two-tone load-pull measurements were carried on the 80W-packaged device. The carrier fundamental frequency is 1950MHz, a spacing of 100KHz is used for the two-tone measurement. Such narrow spacing is chosen to ensure that the system electro-mechanical tuners present almost constant impedance within the 500KHz span covering the two-carrier tones and the left and right IM3 and IM5 intermods. The device is biased in class AB operation, at Vds= 28V and a quiescent current Ids= 1A.

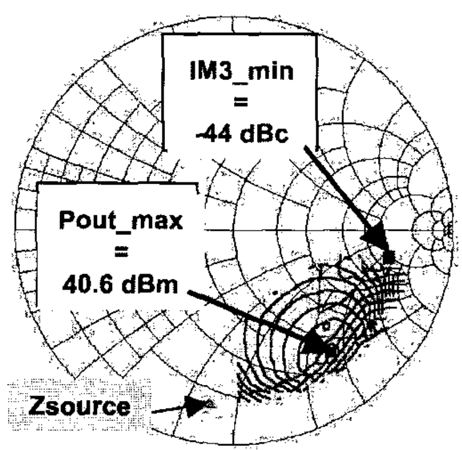

Figure 6: *Measured Power and IM3 contours of the 80W device around 10dB backoff of P1dB; __Power Contours, __ IM3 Contours.*

Power and linearity (IM3, IM5) load-pull contours were measured to obtain the optimum source and load impedances for best power and best linearity device performance. The two-tone load-pull measurement was done at constant input power to deliver output power around 10dB backoff (39dBm) from P_{1dB}. For the sake of clarity, Figure 6 shows the measured contour plots of Pout and IM3 parameters only. Power contours are 0.5dB apart, and IM3 contours are 2dBc apart. An example of model accuracy is given in table 1, where the measured load impedances are compared with simulated ones.

	ZLoad for best Power Tuning	ZLoad for best IM3 Tuning
Measurement	40 – j*90 Ω	240 – j*123 Ω
Model	50 – j*95 Ω	220 – j*150 Ω

Table 1: *Load-pull impedance comparison; Measured vs. Model; Zsource = 9.3 –j*45 Ω*

Figure 7 shows the model prediction vs. measured data of Pout, Gain and PAE as a function of drive level, using the source and load impedance for best power performance obtained from the single-tone load-pull measurement. The same model has been applied using the source and load impedances tuned for a trade-off between linearity and power performance at 10dB backoff from P1dB. The results are shown in Figures 8 and 9, where the model accurately predicts Pout, Gain, drain current, IM3 and IM5 under two-tone operation, over the entire power dynamic range. Usually, for linearity simulation, the model only needs to be accurate in the back-off region.

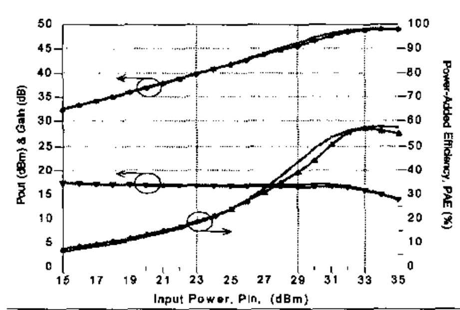

Figure 7: *Model Validation, power, Gain and PAE performance using Source and Load impedances tuned for optimum power and PAE, under single-tone operation __Model, _x_x_Measurement; Zsource = (9.3 – j*45)Ω; ZLoad=(40 – j*90) Ω.*

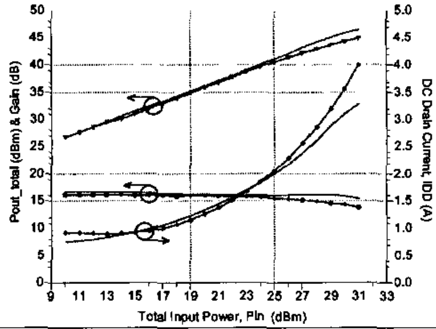

Figure 8: *Model Validation, power, Gain and IDS performance using Source and Load impedances tuned for LINEARITY under two-tone operation, __Model, _x_x_Measurement; Zsource = (9.3 – j*45)Ω; ZLoad=(93 – j*76)Ω*

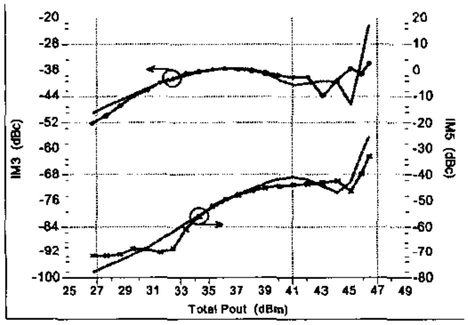

Figure 9: *Model Validation, IM3 & IM5 (worst case) using Source and Load impedances tuned for LINEARITY, __Model, _x_x_Measurement; Zsource = (9.3 – j*45)Ω; ZLoad=(93 – j*76)Ω*

It has been found during the unit-cell model fitting to the IM3 and IM5 measured data that, the modeling of the Cgs characteristic vs Vgs has a crucial role on the accurate prediction of IM3 and IM5 over the entire power dynamic range. In other words, the Cgs model parameters controlling Cgs characteristic shape vs. Vgs and its derivative have to be carefully determined to accurately predict the intermodulation sweet spots and plateau usually found in IM3 and IM5 plot characteristics (see Figure 9).

VI. Conclusion

The paper presented a large-signal model for a packaged 80W device, suitable for 28V GaAs FET high-power technology. The developed multi-cell model achieved very good accuracy in predicting power and linearity performance at the respective optimum source and load impedances obtained from single-tone and two-tone load-pull measurements. This model can be used to speed up the design cycle of higher-power PA modules as well as to optimize the internal pre-matching circuit of discrete packaged transistor devices.

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