MESFET NONLINEARITIES APPLIED TO PREDISTORTION LINEARIZER DESIGN

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ABSTRACT

Three different circuit topologies of predistortion linearizers are proposed using MESFETs biased at low drain bias. The design of a C-band linearizer using two 1 μm gate length devices is detailed and the achieved results compare favourably with conventional designs which use Schottky diodes. The linearizer reduced by 10 dB the intermodulation products of a 10 W power amplifier operating at 6 GHz and up to 4 dB back-off.

INTRODUCTION

The application of predistortion circuits for the linearization of power amplifiers is a must in high density digital microwave systems. This approach results in lower intermodulation levels at the amplifier output so that it can operate at lower back-off values, thus increasing the system efficiency. The papers on linearizer circuits generally use Schottky diodes as intermodulation generators, and varactor diodes as phase shifters for setting the appropriate conditions for intermodulation supression [1,2,3]. Recently, a linearizer employing a MESFET and two varactor diodes has been introduced which presented excellent electrical results [4].

In this paper the main MESFET nonlinearities are explored as sources of intermodulation. Using one of them, three different topologies of predistortion linearizers are proposed consisting only of MESFET devices. This approach presents two advantages compared to previous design: it is cost competitive if employed in a hybrid circuit, and is readily applicable to monolithic design.

MESFET NONLINEARITIES

In a conventional non-linear MESFET model [4], the main nonlinearities are associated with the transconductance, gm, and the output conductance, gd. The former is strongly non-linear when the gate is biased in the vicinity of pinch-off and the latter when the drain is biased at the onset of drain current saturation. Preliminary experiments with the device NE72084, by NEC, showed that the magnitude of the generated intermodulation voltage is essentially the same for both operating conditions. The main difference observed is in the gain behavior, which expands when the device is biased near pinch-off, and compresses when the drain is biased at low voltages. Thus, the bias choice depends on the particular circuit the device is going to be used.

PREDISTORTION LINEARIZER CIRCUITS

In this paper three circuit topologies are proposed, making use of only MESFET devices, associated in a way to control simultaneously the amplitude and phase of the intermodulation voltages. They are designed to match the third order intermodulation, IM_3, characteristics of the power amplifier to be linearized.

TWO DEVICES

This configuration employs two devices paralleled by two 90° hybrids as shown in figure 1. Device A is biased for linear amplification while device B is biased in the non-linear region, at low drain bias, in order to generate the intermodulation component.

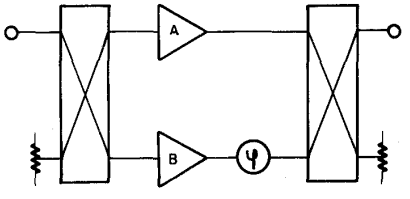

Fig. 1 - Two devices type of linearizer.

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By properly controlling the input power and the drain bias of device B, it is possible to control the magnitude of the intermodulation voltage at the output. The additional intermodulation phase required by the power amplifier is obtained by insertion of a series line in the non-linear path. A low input return loss is expected, since both devices are biased at the same gate bias and presents approximately the same input impedance.

THREE DEVICES

In spite of an increase in the circuit complexity, it is easier to adjust the supression of intermodulation in this configuration. Here, two devices are paralelled as in the first approach, and the association and another linear amplifier is again paralelled with 90° hybrids, as displayed in figure 2. Therefore, devices A and B operate in the linear region, and device C operates in the non-linear region. B and C are adjusted for supression of the linear component, and the resulting intermodulation voltage is added to the linear component from amplifier A.

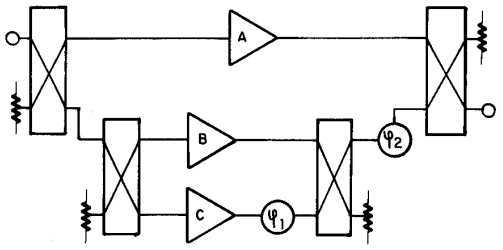

Fig 2 Three Devices type of linearizer.

FOUR DEVICES

The advantage of this configuration is its ability to control the intermodulation phase without changing the delay line.

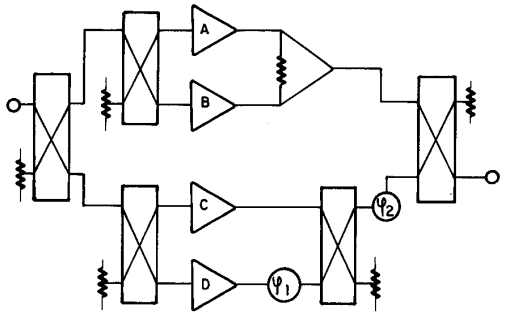

Fig 3 - Four Devices type of linearizer.

The four devices are combined in two blocks as depicted in figure 3. In the first block, devices A and B are combined to act as an active phase shifter. The second block generates the intermodulation as in the previous circuit configuration. Thus, at the output one has a linear component which can have its phase controlled in respect to the non-linear intermodulation component.

TWO DEVICES LINEARIZER DESIGN

A. Basic Concept

The linearizer design starts with the determination of the intermodulation complex voltage generated by the power amplifier. This component is determined from the amplifier AM-AM and AM-PM conversion measurements when excited by a one tone signal. Simple expressions have been developed elsewhere [2] which relate these measurements to the complex intermodulation voltage, using the complex coefficientes of the output voltage expanded in power series.

Then, a linearizer circuit is designed to provide an intermodulation voltage of the same magnitude but opposite phase. The parameters to be determined are the drain bias, V_{DS} , the input power, P_{in} , and the phase shift angle, θ.

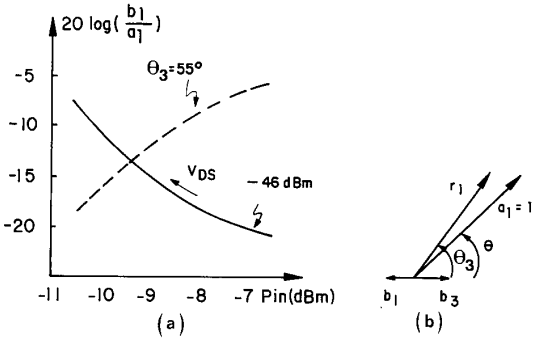

Fig 4 - a. Determination of linearizer parameters;b. Voltage gain phasor diagram

The solution is sought by first considering the magnitude condition for the intermodulation voltage at the output. For that purpose the linear amplifier gain, a_1, and the linear component gain, b_1, of the non-linear amplifier are measured as a function of input power and drain bias. A typical result is plotted in figure 4a. In this measurement, only the values giving the IM_3 required by the power amplifier were retained. It can be observed that for low input power, higher bias is required in order to obtain the desired intermodulation level. Under a certain minimum input power

the circuit becomes uneffective as an intermodulation generator.

The second step, is to find a phase condition for the intermodulation. This can be obtained from the phasor diagram depicted in figure 4b, where b_1 and a_1 add to define the total circuit gain, r_1. The intermodulation component, b_3 , is also represented with a phase θ_3 is respect to r_1. Employing simple geometric relations it can be shown that b_1, r_1 and θ_3 are related by equation 1. The dependence of the input power on b_1 can be obtained by considering the complete unity power gain represented by equation 2.

$$r_1 = -b_1.\cos(\theta_3)+(a_1^2 - b_1^2\sin^2(\theta_3))^{1/2} \quad (1)$$

$$20\log(r_1) = P_{out} - P_{in} \quad (2)$$

Since the output power is constant and determined by the power amplifier requirements, b_1 as a function of P_{in} can be calculated from equations 1 and 2, and the result plotted in figure 4a, as a dotted line. The intersection of both curves gives the solution to the problem. It can be observed from the phasor diagram and equation 2, that higher b_1, implies a reduction in r_1, resulting in higher input power to maintain the constant output power condition. The particular condition $\theta_3 = 0°$, means the gain reduction will be too high, so that this configuration is no more adequate, and it is preferrable to employ the three devices topology.

The phase shift θ, to be introduced in cascade with the non-linear amplifier, is also obtained from the phasor diagram of figure 4b. The calculated delay between the linear and non-linear-paths is given by equation 3.

$$\sin(\theta) = r_1.\sin(\theta_3)/a_1 \quad (3)$$

B. Experimental Prototype

The power amplifier employed in the linearization experiments is capable of delivering 10 W of CW power at C - band with a power gain of 40 dB [5]. This unit requires at the input an intermodulation level of 40 dBC, delayed by 55° at - 7 dBm, for an output power of + 33 dBm.

The realization of the MESFET linearizer starts with the design of the linear and non-linear amplifiers using the device S-parameters. The linear device is biased at V_{GS} = -0.5 V, V_{DS} = 3.0 V and the non-linear at V_{GS} = -0.5 V, V_{DS} = 0.4 V. In this application each amplifier has to be considered as a three port component. Thus, assuming a two tone microwave signal, the input and output ports operates at frequencies f_1, f_2 and f_1, f_2, $2f_2-f_1$, $2f_1-f_2$ respectivelly. The third port corresponds to the drain bias, which operates at the frequency difference f_2-f_1. The behavior of this port is not in general predicted by simplified analysis, and the effect of its termination has to be experimentally determined.

Employing the device NE 72084, the linearizer prototype was constructed on a soft substrate presenting = 6. As shown in figure 5, the amplifiers were paralleled by branch arm couplers and their impedances were matched with open stubs. The circuit area is equal to 25.4 X 30 mm^2.

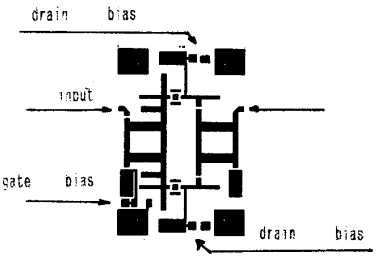

Fig 5 - Mask of the linearizer.

C. Results

Initially, the prototype was cascaded with the power amplifier, and some experiments were carried out to determine the influence of the difference frequency termination. It was found that the suppression of the intermodulation products is strongly dependent on the termination and on the difference frequency, but is less dependent on the particular operating microwave frequency. Thus, one termination may present a very good result at 100 MHz but is poor at 10 MHz. Considering the potential application of this type of linearizer to nQAM modulated carriers, the required instantaneous bandwidth is in the order of 20 MHz. Therefore, this termination was optimized for operation within this bandwidth, and consisted of a high capacitance, equal to 0.1 µF.

The circuit was bias adjusted for mid band operation, at 6175 MHz and the output power of each tone was adjusted for +30 dBm. At this power level the intermodulation products of the power amplifier is - 40 dBC. Introducing the linearizer, the resulting rejection improvement is in the order of 11 dB and at the 500 MHz bandwidth extremes it decreases to 8 dB. The results displayed in figure 6 show that the reduction is constant and

equal to 10 dB up to an output power of + 36 dBm.

The use of the linearizer resulted in an increase in the output power at the 1 dB compression point by 0.2 dB. This characteristic can be improved if the circuit is adjusted at a higher power level.

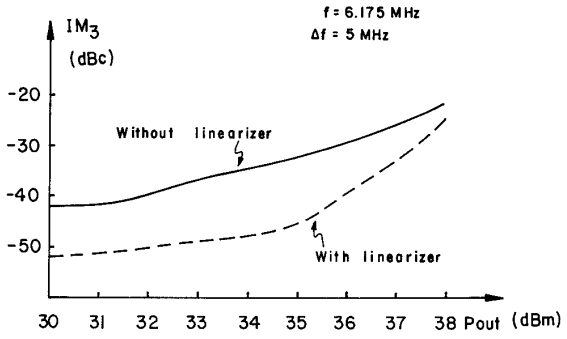

Fig 6 - Linearizer performance.

In figure 7 it is shown the frequency spectrum results for the amplifier with and without linearizer. Each tone measures + 30 dBm and it can be observed an intermodulation reduction slightly greater than 10 dB.

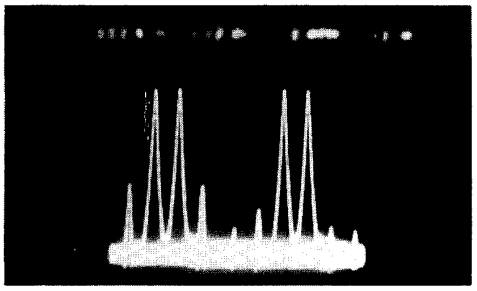

Fig 7 - Amplifier output freq. spectrum
left without linearizer;
right with linearizer.

At higher power the circuit continued to operate but the fifth order products increased and leveled at the third order level. Other important parameters of the linearizer are the input return loss which is better than 10 dB, the total insertion loss which is equal to -0.7 dB and the DC power consumption which is in order of 60 mW.

CONCLUSIONS

An experimental analysis of the MESFET non-linearities was carried out to determine its efficacity as an intermodulation generator. It was verified that the non-linear gm or gd can be used for that purpose. Using gd, three different configurations have been proposed. Similar topologies can be derived for non-linear gm.

The design approach of a simple linearizer employing two low cost MESFET devices was detailed and the circuit was constructed on soft substrate. When cascaded with a C-band 10 W power amplifier, the measured results showed a constant 10 dB improvement up to an output power of + 36 dBm. The prototype also increased the output power by 0.2 dB at the 1 dB compression point.

The obtained performance compares favourably to diode linearizers, presents a higher dynamic range and the resulting prototype is cost competitive. The proposed approach is also adequate for monolithic integration, where the gate area can be independently designed for the linear and the non-linear amplifier, resulting in improved performance compared to hybrid circuit designs.

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