

Reactance compensation matches FET circuits

Transmission line sections smooth impedance paths over medium bandwidths by equalizing reactances at either end of a C-band GaAs MESFET amplifier.

FOR octave-bandwidth GaAs MESFET designs, computer techniques give the best results. But such programs can require considerable time and can be quite tedious. An analytic approach, rather than computer optimization, may therefore be the most desirable method.

A good place to begin the analytic approach is at the active loads. The requirements for matching active loads are stringent. For example, the theorem for maximum power transfer from a synthesized load and a particu-

lar device impedance requires that resistive parts be equal in value. In addition, the reactive elements must also be equal but opposite in sign over the entire frequency band of interest.

Because the impedances of a GaAs MESFET generally can be simulated by series or shunt RLC circuits, an elegant method of matching is to resonate each equivalent circuit at the center frequency, and then, before matching resistive parts, to compensate the reactive slope of each resultant circuit by the reactive slope of its dual.^{1,2} By that means, and depending on the Q factor of the transistor equivalent circuit, bandwidths of 20 percent or greater are possible.

A GaAs MESFET amplifier for 3.7 to 4.2 GHz well illustrates the transmission-line matching technique

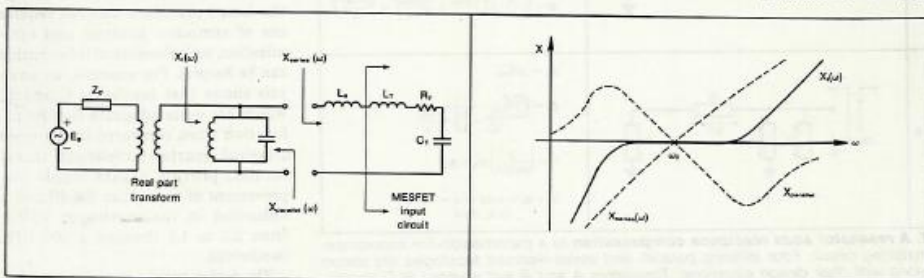
for both shunt- and series-resonant circuits. The amplifier is designed for flat in-band gain and a good input and output VSWR.

To synthesize a matching network for GaAs MESFET input and output impedances, a circuit must be able to transform the real part of the device impedance into the real part of the load. Also, the reactive slope parameter of the resonated device's impedance at the center frequency, $d_x/d\omega$, must be equal to and of the opposite sign of the reactive slope of the transforming-circuit impedance.

A quarter-wavelength transformer readily handles the first requirement, but the second is a bit more difficult. One way to do it is by means of reactance compensation, using circuits that have different resonant impedances. In a lumped-element circuit (Fig. 1), the input impedance of a GaAs MESFET, represented by the $R_T L_T C_T$ circuit, is resonated by an added inductance, L_m . The resulting resistance is transformed to the impedance Z_0 by a wideband transformer. The reactive

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Edmar Camargo and Denise Consoni, Universidade de São Paulo, Laboratório de Microeletrônica, CP. 8174, 01000 São Paulo, Brazil; and Robert Allen Soares, Centre National D'Etudes de Télécommunications, BP 40, 22301 Lannion Cedex, France



1. Inductance L_m added to a lumped-element circuit, helps cancel reactance for better circuit impedance matching.

DESIGN FEATURE

Reactance compensation (continued from p. 93)

component is compensated by a resonant parallel circuit.

Transmission lines can also be used for compensating the reactance simply by adding a series or parallel resonator to a quarter-wavelength transformer. For this technique, several different matching topologies, along with their respective design equations, can be used (Fig. 2). The two most important device parameters in the equations are Q_T , the quality factor of the resonant device impedance, and R_T , the real part of the device's impedance.

Depending on the values of Z_1 and Z_2 , each circuit provides either positive (series-resonant) or negative (parallel-resonant) slope-reactance compensation. However, because of a GaAs MESFET's impedances, the first two

topologies are more suitable for shunting RLC circuits, the second two topologies, series circuits.^{3,4}

The design equations were developed first by an analytical evaluation of the complex impedance of the matching circuit's input. Next, the Q factor is found by using the reactance slope parameter at the center frequency:

$$Q = \frac{\omega_0}{2R} \cdot \frac{dX}{d\omega} \bigg|_{\omega_0} \quad (A)$$

Finally, the Q of the matching network is added and is treated as being equal to but of the opposite sign from the value of the device's impedance at resonance. The resulting equation is solved for Z_1 and/or Z_2 . An analytical evaluation of bandwidth requires calculations of second derivatives, a diffi-

cult task best left to a computer.

To design an amplifier, the transistor's equivalent input and output impedance must first be found from measured S-parameters and circuit theory.⁵ Next, to determine the value of R_T , an external element must be added to resonate the circuit. The transistor's input and output Q_T factor is calculated next, followed by selection of the appropriate topology for a perfect match.

Occasionally, the solution will not be practical because it will not match the capabilities of existing microstrip and dielectric-substrate technology. To avoid a dead-end design path, a series of design graphs corresponding to the four topologies can be used (Fig. 3). The curve parameters, Z_1 and Z_2 , travel within practical limits for commonly used substrates.

An RC parallel circuit with an R_T of 100 Ω and a Q_T of 1.5 is a good example of how the graphs are used. Topology A yields an impedance of 70 Ω for Z_1 and 30 Ω for Z_2 . Topology B produces an impedance close to 40 Ω for the short shunt stub and the same value for Z_1 .

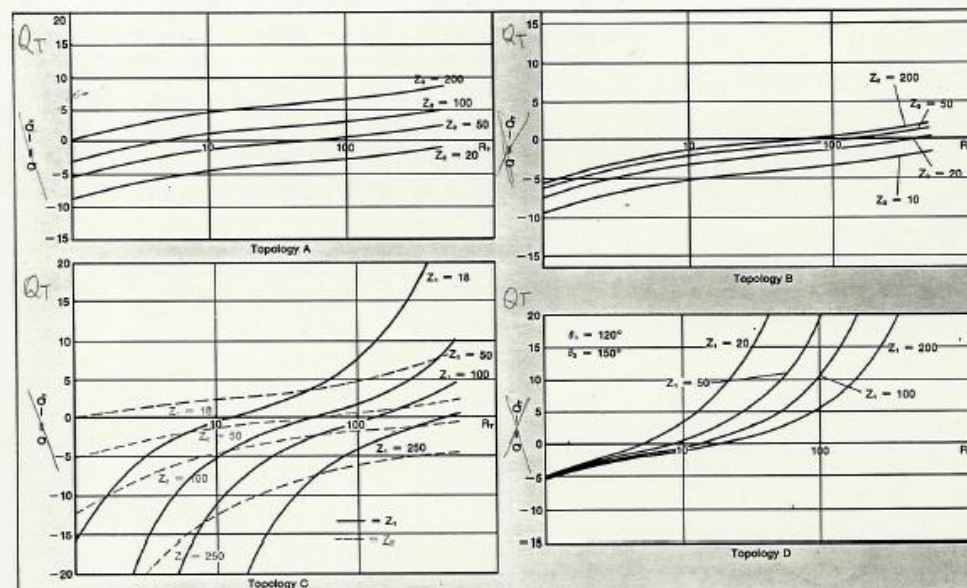
To demonstrate the effectiveness of the matching technique, a one-stage amplifier was designed using an NEC24483 GaAs MESFET. To ensure unconditional stability over the 3.7-to-4.2-GHz range, a 15- Ω series resistor was added to the gate circuit. The bilateral source and load impedances were calculated for a conjugate matched amplifier using conventional circuit theory.

The equivalent input and output impedances dictate a series RC circuit, so high-impedance line sections are used to resonate both circuits at the center frequency, 3.95 GHz. Although the design procedure does not require use of computer analysis and optimization, such theoretical information can be helpful. For example, an analysis shows that topologies C and D, which are quite adequate for the RC function when compared to the more classical quarter-wavelength transformer, provide a gain ripple improvement of more than 0.6 dB and a reduction in the maximum VSWR from 2.3 to 1.5 through a 500-MHz bandwidth.

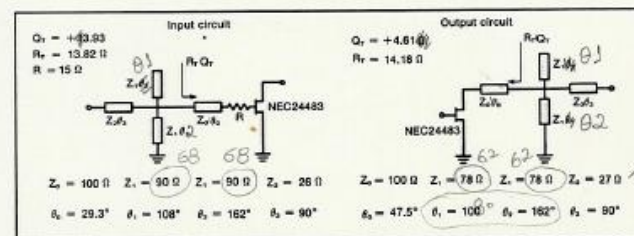
The design graphs show that neither topology C nor topology D can be con-

Topology	Design equations
<p>A</p>	$Z_1 = \sqrt{R_T Z_L}$ $T = \left(\frac{-2Q_1}{r} - \frac{1}{2} \left(\frac{Z_L}{Z_1} - \frac{Z_1}{Z_L} \right) \right)$ $Z_2 = \frac{-TZ_1}{2} + \sqrt{\left(\frac{TZ_1}{2} \right)^2 + Z_L^2}$
<p>B</p>	$Z_1 = \sqrt{R_T Z_L}$ $Z_2 = \frac{\pi Z_L Z_1^2}{\pi Z_1^2 - \pi Z_L^2 - 4Q_1 Z_L Z_1}$
<p>C</p>	$Z_1 = AZ_L$ $Z_2 = BZ_L$ $A = \sqrt{R_T/Z_L}$ $B = \left(\frac{A}{1+A} \right) \left(\frac{-2Q_1}{r} + \sqrt{\left(\frac{2Q_1}{r} \right)^2 + \left(\frac{1+A^2}{A} \right)^2} \right)$
<p>D</p>	$Z_1 = \sqrt{R_T Z_L}$ $Z_2 = \frac{1}{\left(\frac{1}{Z_L} - \frac{1}{Z_1} \right) + \frac{4Q_1}{r}}$ $T = \left(\frac{2}{r \cos^2 \theta_1} \right) (\theta_1 + \theta_2)$ $\theta_1 + \theta_2 = \pi n/2 - n = \pi \text{ or } 3$ $\theta_1, \theta_2 \text{ in rad}$

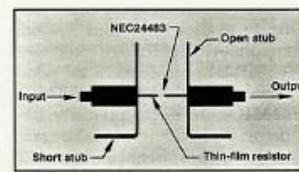
2. A resonator adds reactance compensation to a transmission-line impedance-matching circuit. Four differing parallel- and series-resonant topologies are shown along with their design equations. Topologies A and B suit shunted RLC circuits, and C and D series types.



3. Design graphs help determine the suitability of a substrate type for a particular topology. The matching impedance values, Z_1 and Z_2 , are appropriate for microstrip lines on popular dielectric substrates.



4. A suitable impedance match for an NEC24483 GaAs MESFET using topology D requires the component values shown. The quality factor of the device's impedance, Q_T , as well as the real part of the impedance, R_T , must be determined before use of the design equations.



5. A mask shows the suitable microstrip circuit for matching a GaAs MESFET amplifier's input and output impedances.

constructed on a soft substrate because of the required circuit dimensions. However, by varying the value of parameter T , the electrical lengths of the stubs used for topology D can be modified to create the correct impedance for Z_1 . Parameters R_T and Q_T for the project, along with the final parts values for topology D input and output matching circuits, are shown in Fig. 4. The mask used for fabrication of the circuit on a

soft substrate is shown in Fig. 5.

Measured circuit characteristics closely match those predicted by computer simulations. For example, in-band gain is 11.0 ± 0.1 dB and return losses are about 20 dB. ••

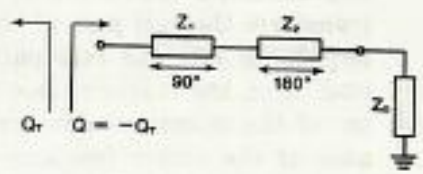
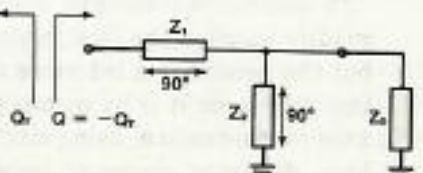
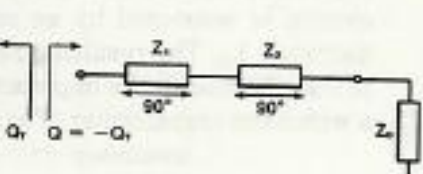
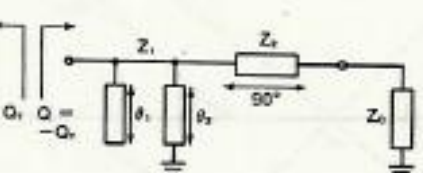
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Corrected Equations

	Topology	Design equations
A		$Z_1 = \sqrt{R_T Z_o}$ $T = -\frac{2Q_T}{\pi} - \frac{1}{2} \left(\frac{Z_o}{Z_1} - \frac{Z_1}{Z_o} \right)$ $Z_2 = -\frac{TZ_o}{2} + \sqrt{\left(\frac{TZ_o}{2} \right)^2 + Z_o^2}$
B		$Z_1 = \sqrt{R_T Z_o}$ $Z_2 = \frac{\pi Z_1 Z_o^2}{\pi Z_1^2 - \pi Z_o^2 - 4Q_T Z_1 Z_o}$
C		$Z_1 = AZ_2 \quad Z_2 = BZ_o$ $A = \sqrt{\text{Re}(Z_T) / Z_o}$ $B = \frac{A}{1+A} \left\{ -\frac{2}{\pi} Q_T + \sqrt{\left(\frac{2}{\pi} Q_T \right)^2 + \frac{(1+A)^2}{A}} \right\}$
D		$Z_2 = \sqrt{R_T Z_o}$ $T = \frac{2}{\pi \cos^2 \theta} (\theta_1 + \theta_2)$ $Z_1 = \frac{TZ_2^2}{Z_o} \frac{1}{\left(\frac{Z_o}{Z_2} - \frac{Z_2}{Z_o} \right) + \frac{4Q_T}{\pi}}$

2. A resonator adds reactance compensation to a transmission-line impedance-matching circuit. Four differing parallel- and series-resonant topologies are shown along with their design equations. Topologies A and B suit shunted RLC circuits, and C and D series types.

$$(\theta_1 + \theta_2) = n\pi / 2 \rightarrow n = 1, 3$$

$$\theta_1, \theta_2 \quad \text{In rd}$$