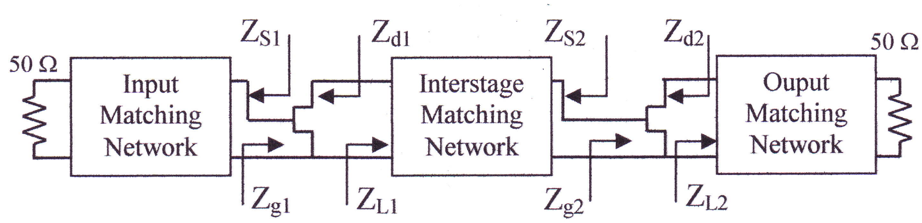
Amplifier Notes

Millimeter Wave GaN Power Amplifier Design

LNA

The question of designing a core amplifier for a LNA following the same methodology employed in the design of a power amplifier, is as follows. In the PA, the load impedance is designed for either power, efficiency or linearity. The ISMN is designed for best match of the output stage gate impedance. That will allow the PA to achieve highest gain delivering its best power and efficiency. In the LNA the source impedance is designed to match the optimum source termination for best noise figure. The ISMN has to provide a termination to the drain of the first stage to maximize its power gain, condition where the first stage also delivers its best noise figure. The matching for the second stage gate is a second priority.



Errata

In spite of several revisions of the book, I received information on an error detected on equations 2.7 and 2.8. The correct equation is shown below where h_{norm} is a normalization factor equal to 100 µm, and h is the substrate thickness in µm

$$R = 0.125 \frac{h}{h_{norm}} \text{ in ohm} \qquad (2.7)$$

$$L = 14 \frac{h}{h_{norm}} \text{ in pH} \qquad (2.8)$$

Thermal considerations

This topic was left out of the book, because until recently this task was usually left for the mechanical or process engineers. Now it is considered part of the MMIC design package. We start with the power dissipated in a MMIC amplifier, given by the equation below. In general, if the device power gain is higher than 6 dB one can just disregard the contribution of the input power, P_{in}. However, at power gain levels below this value, it has to be considered. For instance, in the limit of 3 dB gain, the input drive becomes equal to 50% of the output power.

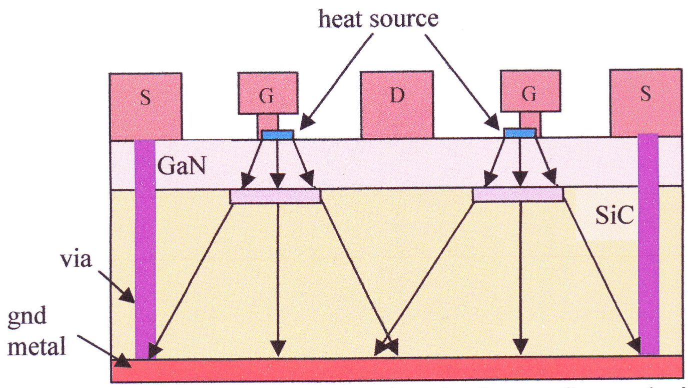
$$P_{diss} = P_{DC} + P_{in} - P_{out}$$

For normal operation, qualification, and reliability, the device channel temperature has to be under a maximum value, specified for a given technology and operating environment. Conventional GaAs FETs are allowed to operate up to 175°C. On the other hand, GaN devices can operate at higher voltage and current densities, and higher RF power is obtained from a smaller device periphery. However, the higher concentration of power means a higher power dissipation, causing the temperature of the device channel to rise more when compared to GaAs. The maximum channel temperature for GaN is in general set at 150°C. Therefore it is important to estimate the junction temperature from a MMIC power device at the design phase. The channel temperature is described by the next equation.

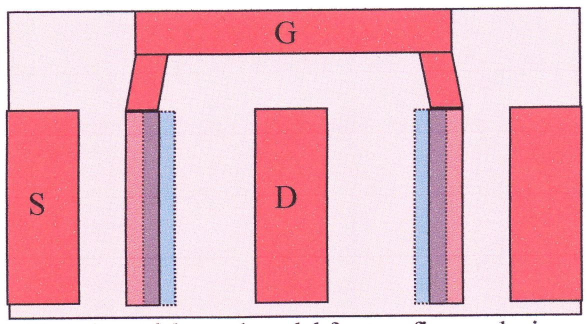
$$T_{ch} = T_{ref} + R_{th} P_{diss}$$

with T_{ch} = channel temperature
T_{ref} = reference temperature at the base plate
R_{th} = thermal resistance

The thermal resistance parameter can be measured directly from the device. Therefore, most design houses accumulate experiences after a few design iterations and are able to deliver MMICs capable of reliable operation. However, for a priori estimate a simulation process should be employed. The MMIC design engineer should prepare a layout model of his power devices, specifying a two-dimensional uniform heat source, layered on top of the hot spots. Simulations[1] indicate the hottest area is near the gate on the drain side, indicating the heat source should be applied next to the gate on the drain side. The heat source width is equal to gate width, while the length can be larger than the gate, usually between 0.5 to 1 μm. An illustration of the layout model for thermal analysis is shown in the figure below. The arrows indicate an idealistic path for the heat flow.



Cross section view of thermal model for two fingers device



Top view of thermal model for two fingers device

[1]J. Li, and J. Mao, "Analytical Thermal Model for AlGaN/GaN HEMTs Using Conformal Mapping Method, "IEEE Transactions on Electron Devices, Vol. 69, No 5, May 2022, pp 2313 - 2318

At this point there are two defined temperatures, at the bottom, corresponding to the T_{ref} and at the top corresponding to the P_{diss} on each finger. To find the temperature distribution, the heat flow simplified equation[2] indicated below, is solved numerically. Finite element method (FEM) and finite difference method (FDM) software packages and electro thermal tools are used to find the temperature distribution in the channel. From the thermal conductivity the thermal resistance R_{th} is then determined.

$$\nabla \bullet \left(k \nabla \theta(r,t)\right) + P_{diss} = 0$$

Where k is the thermal conductivity

θ is the temperature as a function of position r and time t

There are many software packages on the market that can solve the thermal flow equation. Recently, major software houses embedded such software with the circuit simulation software, so that one can find a more accurate power performance considering the device temperature. To my knowledge Keysight, Cadence_AWR and Ansys are the companies providing such a complete solution.

[2]Y. Takahashi, R. Ishikawa, and K. Honjo, "Precise Modeling of Thermal Memory Effect for power Amplifier Using Multi-Stage Thermal RC-Ladder Network," 2006 Asia-Pacific Microwave Conference

Some of the parameters required for thermal simulations are in the table below, obtained from a recent publication[3].

Material	Dielectric Constant	Thermal Conductivity	Specific Heat	Thermal Diffusivity	Mass Density
	Er	k [W/(cmK)]	cp [J/(gK)]	D [cm^2/s]	ρ [g/cm^3]
GaN	10.2	1.5	0.68	0.385	6.11
SiC	9.7	4.2	0.24	4.673	3.21

[3]T. Kang, Y. Ye, Y. Jia, Y. Kong, and B. Jiao, "Enhanced Thermal Management of GaN Power Amplifier Electronics with Micro-Pin Fin Heat Sinks, "Published by www.mdpi.com/journal/electronics October 2020