AN EFFICIENT DESIGN APPROACH FOR MESFET AND HEMT FREQUENCY DOUBLERS

Fatima S. Correra and Edmar Camargo

Laboratório de Microeletrônica
Universidade de São Paulo
P.O. Box 8174, CEP 01051, São Paulo - BRAZIL

ABSTRACT

A simple and accurate design method for frequency doublers combining linear and non-linear analysis is presented. This approach was applied to study the optimum bias and to compare the performance results of MESFET and HEMT frequency doublers. The theoretical predictions were verified experimentally on a 6 to 12 GHz frequency doubler that exhibited multiplication gain of 10.5 dB for a 0.3 μm gate length HEMT and 8.5 dB for a MESFET with approximately the same gate dimensions.

INTRODUCTION

In general, frequency doublers are obtained by biasing the gate near pinch-off and exploring the harmonic content of the drain current. In order to obtain an efficient frequency doubler in terms of output power and multiplication gain, the appropriate large-signal impedances must be connected at the drain and gate at several harmonic frequencies. Two important methods of determining the large-signal impedances have been published: the first[1] employs an automatic step by step matching of the input and output MESFET impedance as the generator increases its amplitude, and the second[2] employs an optimization algorithm for maximum output power and minimum input power, directly derived from terminal voltages and currents constrained to the physical reality of the synthesized impedances.

The purpose of this paper is to present an efficient and simple design method for frequency doublers employing MESFETs and HEMTs. Some laboratory experiments were carried out with these devices to corroborate the theoretical predictions, and the results are presented in a comparative way.

NON-LINEAR DESIGN APPROACH

Figure 1 shows the non-linear equivalent circuit used to represent the MESFET and the HEMT. The non-linearities considered are the input capacitance $C_{GS}(V_{GS})$ and the drain current source $I_D(V_{GS},V_{DS})$. The dependence of these elements on the gate-source and drain-source voltages are presented at references 3 and 4 for HEMT and MESFET, respectively.

The design approach proposed in this paper starts with the analysis of the interaction between a simplified non-linear transistor model and an external hypothetical circuit. As depicted in figure 2, the transistor model is composed by the input capacitance and its charge resistance and by the drain current source shunted by the output conductance. In this model feedback and parasitic effects have been neglected, improving simulation efficiency. For maximum generation of harmonics the transistor gate is biased near the pinch-off voltage and the output load is a short circuit at all frequencies to provide efficient modulation of the drain current. The FET input circuit is conjugately matched to the generator to maximize the voltage excursion on the input capacitance. The input circuit parameters, including the RF generator amplitude at the fundamental frequency, the average value of the non-linear capacitance and the drain current waveform are determined iteratively by carrying out non-linear simulations. In the present context, the time domain simulator SPICE was employed to perform this task.

The second step of the design method is the determination of the optimum second harmonic load, which is considered to be resistive in this model. It is obtained by the relation between the maximum dynamic drain voltage and the second harmonic content of the clipped drain current. The dynamic drain voltage depends on drain bias and on the device I_{DS} x V_{DS} characteristics. Thus, drain voltages are assumed to be zero at all frequencies except at the second harmonic. The resulting harmonic voltages and currents are then transferred to the device external terminals, employing the complete transistor model and simple linear transfer equations[5]. The external voltages and currents are then used to synthesize the large-signal impedances and to calculate the multiplication gain and the power distribution at the several harmonics.

This procedure does not take into account the harmonic voltages present at the input circuit due to feedback effects. In general, they can be neglected if their amplitude are much lower than the fundamental voltage. However, if this is not the case, a refinement in the design can be made by adding to the fundamental frequency generator of the simplified circuit, a second harmonic generator with an amplitude determined by the feedback introduced by the transistor parasitics. The entire procedure is then repeated for this new gate voltage and the new harmonic currents and voltages are transferred to the external terminals.

The full application of this approach requires matching the transistor external terminals at all harmonics, in order to guarantee that the internal voltages and currents remain as initially proposed. Of course, this is very difficult if not impossible, so the number of harmonics must be limited. However, the usual practice of considering only the fundamental and second harmonic frequencies in the case of doublers, results in small interference on the shape of the drain current waveform, and can be adopted with acceptable results.

SIMULATION RESULTS

In order to give support to the design method presented, two transistors possessing the same gate area 0.5x300 μm^2 and similar RF characteristics have been modelled - the HEMT 2SK677 by SONY and the MESFET NE70083 by NEC.

A first set of simulations were carried out at low frequencies, to investigate the optimum bias for efficient harmonic generation. The second harmonic content of the clipped drain current waveform depends on gate bias. This dependence is better explained by the device conduction angle[2], defined by equation 1, as a function of gate bias V_{GS}, pinch-off voltage, V_P, and by the amplitude of the dynamic input voltage, V_o.

$$\cos(\phi/2) = (V_{GS} - V_P)/V_o \qquad (1)$$

Figure 3 displays the percentage of second harmonic compared to the drain current peak as a function of the conduction angle for both types of transistors. Observation of this figure indicates that the best conduction angle for the MESFET is 120^o, a result which has already been pointed out in a previous publication[2]. However, in the case of HEMTs, the maximum second harmonic percentage occurs for a conduction angle around 160^o, remaining approximatelly constant between 120^o and 180^o. Then, 180^o can be considered an adequate conduction angle for the HEMT, since class B operation eases the input matching requirements. Thus MESFET doublers requires class C bias for efficient operation, while HEMT doublers can operate at class B with high performance. The choice of optimum drain bias requires a consideration on the expected voltage excursion over the $I_{DS} \times V_{DS}$ plane and on the limits imposed by the device avalanche breakdown voltages.

A second set of simulations were made to analyse the influence of transistor parasitics, bonding wires, and package parasitics on the frequency doubler performance. A 7.5 to 15 GHz frequency doubler was simulated using the simplified transistor model for the HEMT 2SK677, biased at 180^o. Its performance was evaluated for three different circuit implementations namely, monolithic circuit, hybrid circuit employing chip transistor, and hybrid circuit with package device. The monolithic approach, for which only parasitic capacitances and resistances are aggregated to the device, results in a multiplication gain of 16 dB. The application of the chip device in a hybrid circuit where typical bonding inductances ($L_G = L_D = 0.2nH$; $L_S = 0.12nH$) are taken into account, decreases the gain to 8.5 dB. Finally, the packaged device is assumed to be used, resulting in a gain of 8 dB. The simulations indicated that second harmonic power remains essentially constant with a 0.5 dB decrease from the maximum value of +9.5 dBm at the monolithic level to +9 dBm at the package level.

EXPERIMENTAL RESULTS

A frequency doubler for the 6 to 12 GHz frequency band was designed by this approach using the HEMT 2SK677. The theoretical predictions indicated a multiplication gain of 9.4 dB for an input power of -2 dBm and a maximum output power of + 9.6 dBm for an input power of + 1 dBm. An experimental test circuit was implemented on 0.635 mm thick alumina substrate and its topology is represented in figure 4. The drain circuit consists of an harmonic filter cascaded with a small reactance to match the second harmonic impedance. The filter is composed by a set of 90^{o} open stubs at the fundamental frequency, which blocks the fundamental and third harmonic and are transparent at the second harmonic. The input circuit employed 45^{o} open stubs at the fundamental frequency which reflect the second harmonic to the gate, and simultaneously matches the fundamental frequency.

Initially, the HEMT 2SK677 was inserted in the test circuit, biased at a conduction angle of 180^{o} and adjusted for best performance. The resulting position of the stubs followed closely the theoretically predicted impedances. The measured multiplication gain as a function of input power is presented in figure 5. It was obtained maximum multiplication gain of 10 dB and maximum output power of +8.5 dBm, comparing favourably with the predicted results.

The same 6 to 12 GHz test circuit was used to verify experimentally the doubling properties of 3 other types of packaged devices, and their results are listed in table I.

		Multiplication Gain-dB		Output Power-dBm	
		measured	simulated	measured	simulated
HEMT	2SK677*	10.0	9.4	8.5	9.6
MESFET	NE70083*	8.0	7.0	8.0	8.5
HEMT	NE32083A**	10.5	-	9.0	-
MESFET	NE71083**	8.5	-	8.0	-

Table I Frequency doubler results for typical HEMTs and MESFETs. Gate length: * 0.5 μm; ** 0.3 μm.

The output power indicated in table 1 was measured with the MESFETs biased at 120^{o} and the HEMTs at 180^{o}. Different conduction angles were tried for the HEMTs and it was experimentally confirmed that 180^{o} is the most appropriate for the present application. It is expected that this conclusion could be extended to devices that shows similar $I_{DS} \times V_{GS}$ characteristics. Comparing the MESFETs with the HEMTs, one concludes that the latter presents a 2 dB higher multiplication gain, and approximately the same output power.

CONCLUSIONS

A design method for frequency doublers which greatly simplifies the non-linear simulations and yet is accurate has

been presented. The experimental results obtained with a test circuit showed a high degree of correlation between predictions and measurements, emphasizing the validity of the design approach. Comparison of MESFETs and HEMTs operation revealed that their optimum conduction angles are different, and that the latter presents at least 2 dB higher multiplication gain. As a matter of fact this high gain at these frequencies for a packaged device can be compared to best published results for dual gate GaAs MESFETs[6] frequency doublers.

ACKNOWLEDGEMENTS

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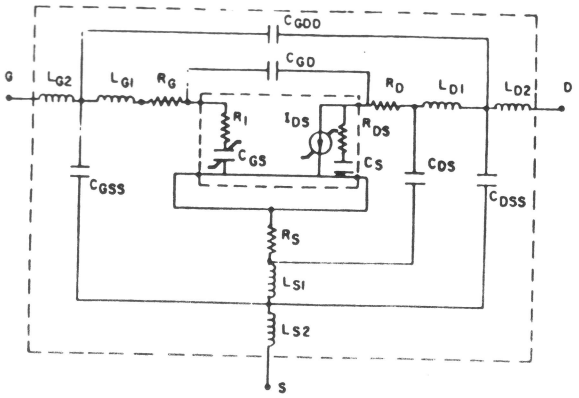

Fig. 1 FET non-linear equivalent circuit.

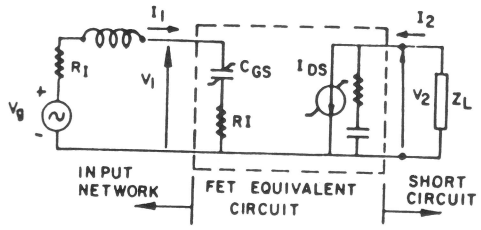

Fig. 2 Simplified frequency multiplier prototype.

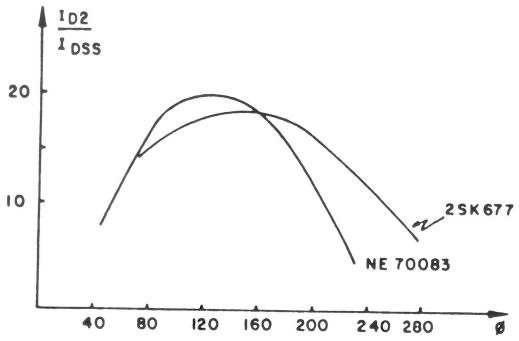

Fig.3 Second harmonic normalized amplitude as a function of the conduction angle.

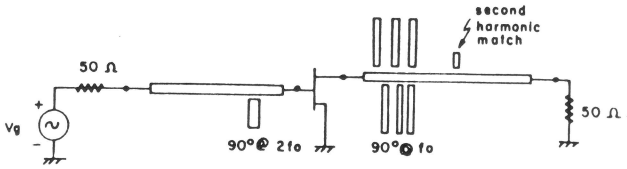

Fig. 4 Test circuit for the 6 - 12 GHz doubler.

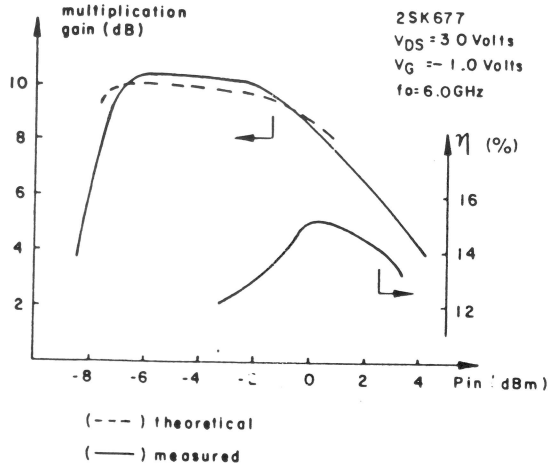

Fig. 5 Multiplication gain versus input power.

B/A depends on fewer components compared to the feedforward, if the amplifier is designed using thin film miniaturized or monolithic amplifier modules. These modern components present small phase shift in its transfer characteristics and their small dimensions result in a short feedback path with acceptable phase shifts for the usual communication frequency bands.

The predistortion technique can be applied to existing amplifiers so that the predistortion circuit can be designed independently and cascaded in front of the main amplifier. Thus, the compensating circuits operate at low levels with low power consumption and with no additional power losses at the output. It is also potentially applicable to a broader bandwidth compared to the previous methods, since the ratio B/A depends only on the performance of three components. Besides that advantage, the predistorter can be independently designed to match the frequency characteristics of the power amplifier. However, since the predistorter is adjusted for a particular output power, it fails to perform for systems that have amplitude variations such as SCPC or SSB-AM. Another drawback of this system is its inability to follow the power amplifier characteristics in a wide temperature range.

In conclusion, it has been shown that the linearizing systems can effectivelly reduce the intermodulation products and a practical means for comparing the performance of different systems has been introduced. It is expected that this paper could be useful as a guide, when deciding which is the most adequate system for a specific application.

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