ULTRAWIDE-BAND MICROWAVE AMPLIFIER WITH PACKAGED GaAs MESFETs

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ABSTRACT

An ultrawide-band microwave amplifier design using packaged MESFETs and soft substrates is presented. Bandwidth limitations are discussed and a two-stage lossy matched amplifier design using low-frequency analysis and computer simulation techniques is detailed. Experimental results are in good agreement with the computed performance and 17 ± 1 dB gain with associated input/output VSWR less than 2 were obtained over 0.1 to 4.6 GHz.

INTRODUCTION

The availability of high transconductance GaAs MESFETs has made possible the design of ultrawide-band microwave amplifiers employing chip transistors, which present high power gain from hundreds of MHz up to frequencies higher than 12 GHz[1,2,3]. However, the application of packaged transistors for this purpose has not yet been explored, mainly due to the limitation imposed by the parasitics at high frequencies. The present investigation focuses on the design of an ultrawide-band amplifier and on the realization trade-offs employing discrete components and microstrip lines on soft substrates.

THEORETICAL DESIGN

A first step in the design regards the transistor selection. The 1 μm gate packaged device NE 21889 (NEC) was considered an adequate choice for the present application, for its low cost and RF performance. Its main characteristics are given as follows: f_{max}= 60 GHz, MAG = 16.5 dB and P_{out} = +15 dBm at 4 GHz.

The next step is the identification of the design goals. The purpose of this work was to explore the bandwidth capability and associated power gain performance of packaged MESFETs. In order to ease the cascading of amplifier modules the following additional design goals are required: input and output VSWR lower than 2 and gain ripple lower than 2 dB. These specifications can be met by single ended feedback or lossy matched amplifiers[2,3]. The latter structure has been chosen since fewer parasitics are involved in the circuit realization.

The final step is the use of a systematic design procedure which consists of a low-frequency analysis followed by computer simulations over the entire bandwidth, applied to the single-ended lossy matched amplifier.

LOW-FREQUENCY ANALYSIS

The topology for the single-stage lossy matched amplifier is shown in figure 1(a). A low-frequency unilateral MESFET model was used to calculate the amplifier power gain, G_1, and the input and output impedances, Z_{in} and Z_{out}. These are expressed in equations (1), (2) and (3) as functions of the transistor parameters, g_m and g_d, the external resistors, R_{in} and R_{out}, and the generator and load impedance, R_o.

$$G_1 = \left[2.g_m \cdot \frac{R_{in}.R_o.R_{out}}{(R_{in} + R_o).[(1 + R_o.g_d).R_{out} + R_o]} \right]^2 \qquad (1)$$

$$Z_{in} = R_{in} \qquad (2)$$

$$Z_{out} = \frac{R_{out}}{1 + g_d.R_{out}} \qquad (3)$$

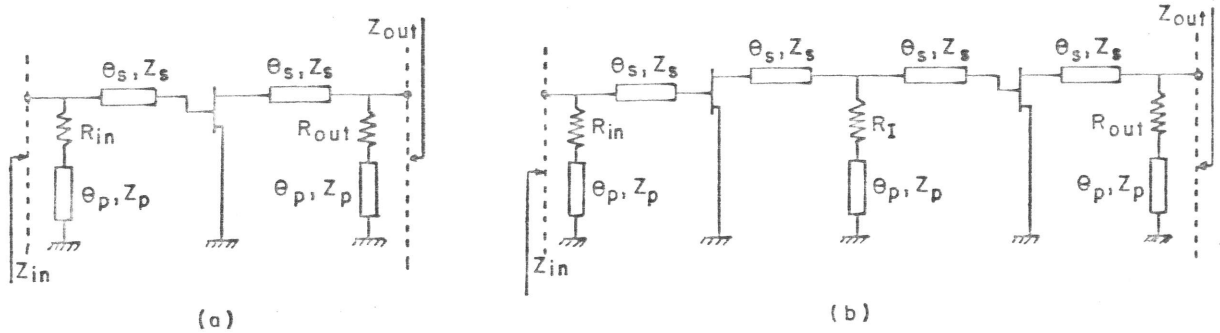

Figure 1 - Circuit topologies for the amplifier (a) single stage; (b) two stages.

From equations (1) to (3) it can be noticed that the matching level and the power gain can not be arbitrarily chosen. This limitation can be overcome by using the two-stage amplifier structure of figure 1(b). In this case the amplifier impedances are still given by equations (2) and (3), but the power gain, G_2, given by equation (4), can be independently adjusted by a proper choice of the interstage resistor, R_I. Additionally, equations (4) reveals that for conventional MESFETs the two-stage amplifier offers a higher gain, when compared to two single cascaded stages indicating that the former structure is the best choice when high power gain is desired.

$$G_2 = G_1 \cdot \left[\frac{g_m.R_I}{1 + R_I.g_d} \right]^2 \qquad (4)$$

HIGH-FREQUENCY ANALYSIS

The gain of the two-stage amplifier of figure 1(b) was calculated from 0.1 to 8.0 GHz using transistor's S-parameters furnished by the manu-

facturer and is represented in figure 2. The set of curver A represents the power gain for matched input (R_{in} = 50Ω), output VSWR of 1.5 (R_{out}= 100Ω) and for two values of the interstage resistor. In this case the transmission lines were neglected ($\theta_s = \theta_p = 0^0$). These curves reveal that resistor R_l has a great impact on the low frequency gain, but becomes less important at high frequencies where it is shunted by the transistor's input impedance.

In the set of curves B, the effect of the transistor's bonding pads were taken into account. Measuring approximately 0.6 x 1.0 mm, they can be represented as short lenghts of transmission lines (Z_s = 100Ω, $\theta_s = 10^0$ at 6 GHz) on the soft substrate used (ε_r = 2.5, thickness = 0.025"). A gain improvement of 2 dB can be observed at high frequencies, as well as a fall-off above 6 GHz due to the interaction between the inductive series lines and the transistor's impedance.

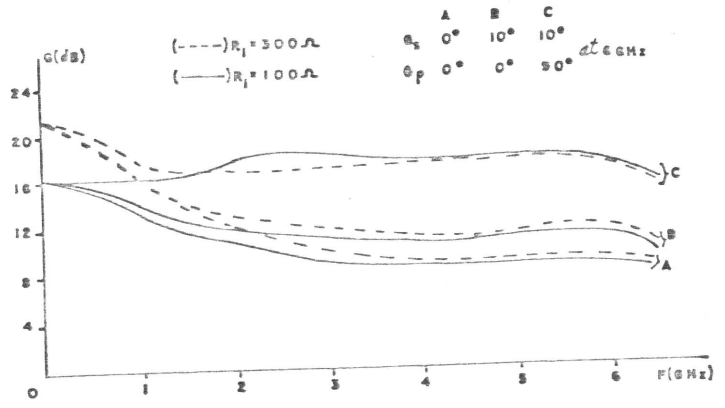

Figure 2 - Computed gain curves for two stage amplifier

Finally, the set of curves C shows the effect of short circuited stubs (Z_p = 100Ω; $\theta_p = 90^0$ at 6 GHz) added in series with the RF resistors in order to improve the gain. The resulting average gain improvement of 4 dB at high frequencies and the flat power gain response observed for R_l = 100Ω, show that this structure represents a good compromise for the amplifier design.

CIRCUIT CONSTRUCTION

The practical circuit realization requires the use of DC block capacitors which must be carefully modelled for use on the final circuit optmization. Thus, an investigation was made on different capacitor types to determine the most appropriate for the above purpose. A multilayer chip capacitor was chosen which series resonate at 1.2 GHz and is modelled as R = 0.2Ω; C_1 = 52 pF and L = 0.35 nH. The stubs are RF shorted to ground by high value chip capacitor(C_2 = 390 pF) mounted through the substrate and bonded onto the ground plane. The other components were surface mounted employing conventional printed circuit bonding techniques. Thin film chip resistors were used providing also bias paths for the transistors. The complete amplifier schematic is depicted in figure 3, and its theoretical performance is

illustrated in the next section. The microstrip lines represented in the figure are 100Ω characteristic impedance and the electrical lenghts were calculated for 6 GHz.

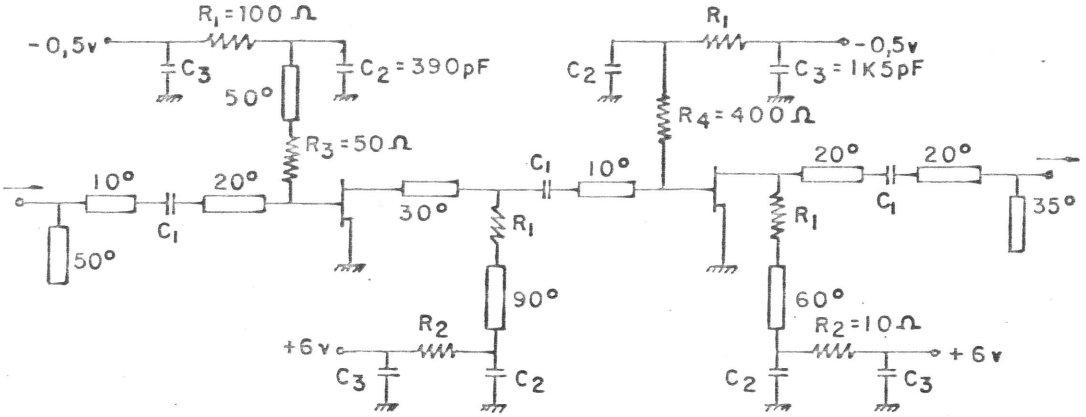

Figure 3 - Amplifier schematic

The complete circuit, measuring 1 x 1.2 inches, was assembled between two SMA launchers and its photograph is shown in figure 4.

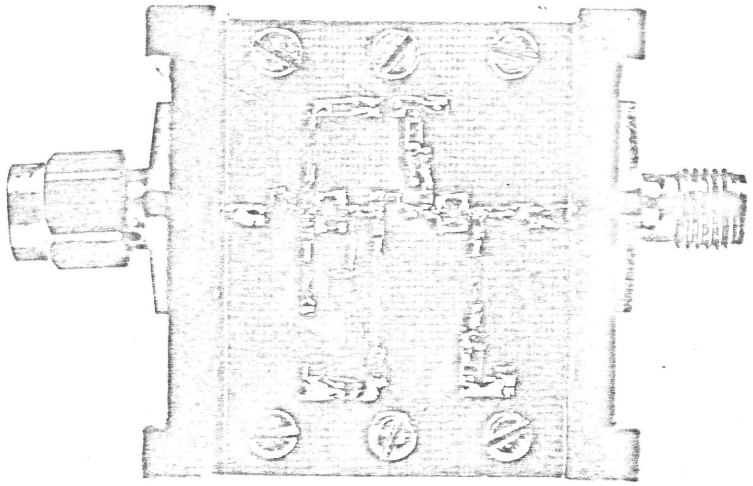

Figure 4 - Photograph of the amplifier prototype

EXPERIMENTAL RESULTS

The amplifier power gain performance measured for V_{DS} = 3 V and I_{DS} = 20 mA is represented in figure 5. A good agreement can be observed with the theoretical predictions. The unit exhibits a power gain of 17 dB and the gain ripple is within ± 1 dB from 0.1 to 4.8 GHz. The noise figure results are also shown in figure 4 with a maximum of 8 dB at 0.1 GHz.

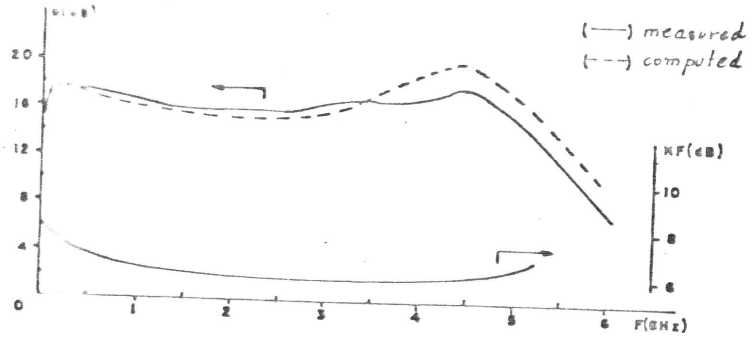

Figure 5 - Small signal power gain and noise figure performances.

The measured input and output VSWR's are depicted in figure 6, which reveals a maximum of 2 at the input and of 1.7 at the output from 0.1 up to 4.6 GHz. The discrepancy with respect to the computed results at high frequencies was expected, since it is extremelly dificult to properly simulate all the parasitic effects. The measured output power at 1 dB gain compression is + 13 dBm for the worst case within the band.

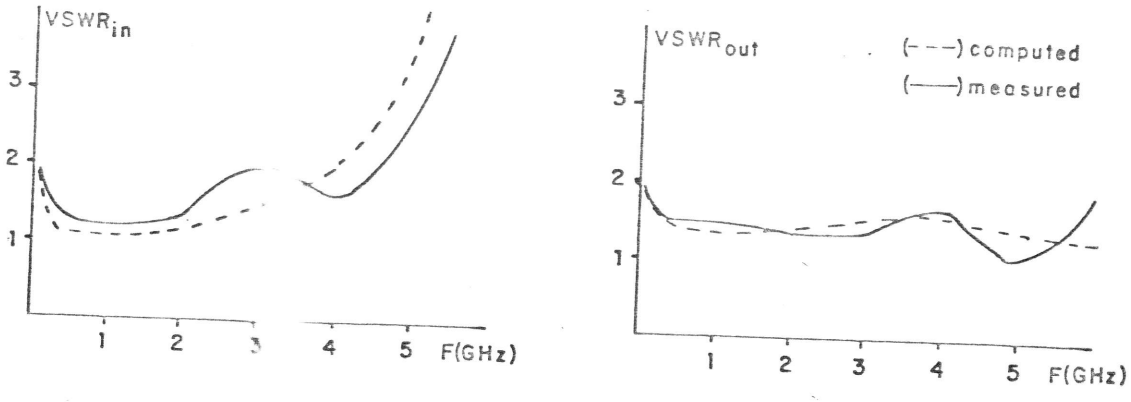

Figure 6 - Amplifier VSWR characteristics

CONCLUSIONS

A two-stage amplifier was designed based on a low-frequency analysis followed by computer simulations. Attention was particulary paid to the choice of the transistor, the multilayer capacitors, the RF resistors and to a careful but simple method of circuit construction. The unit presented a gain of 17 $\pm$ 1 dB over the frequency band of 0.1 to 4.6 GHz representing nearly 5 1/2 octaves of bandwidth and a maximum noise figure of 8.0 dB.

This paper demonstrates that an ultrawide-band amplifier can be obtained and easily reproduced, employing packaged transistors and low - cost printed circuit technology.

ACKNOWLEDGEMENTS

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